College Code - TP

SIDDHARTHA

INSTITUTE OF ENGINEERING & TECHNOLOGY

(Approved by AICTE & Affiliated to JNTU)
Vinobha Nagar, Ibrahimpatnam, Ranga Reddy Dist – 501 506, Telangana, INDIA.
Ph: 08414-222299, 222599, Fax: 08414-222399
E-mail:info@siddhartha.ac.in; www.siddhartha.ac.in

COURSE FILE FOR

PULSE AND DIGITAL CIRCUITS

PREPARED BY

Mr.T.KRISHNARJUNA RAO
M.TECH, (PH.D), FIETE.

ASSOCIATE PROFESSOR
CELL: +91-9010964679
E-mail: krishna410@gmail.com

DEPARMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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COURSE FILE INDEX

S.NO TITLE

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Ranga Reddy District-501 506.

12. QUESTION BANK

12.1 UNIT WISE SHORT QUESTION

12.2 UNIT WISE LONG QUESTIONS

12.3 UNIVERSITY QUESTION PAPER

13. LECTURE NOTES

13.1 UNIT WISE LECTURE NOTES

UNIT-1 : Linear wave shaping

1.1	Response of high pass RC circuit for sine, pulse
1.2	Step and square and ramp response
1.3	Low pass ,sinusoidal and step response
1.4	Square and Ramp response
1.5	RC Differentiator, Integrator
1.6	Attenuators and its applications as a CRO probe
1.7	RL and RLC Circuits and their Response for Step, Ringing Circuit
1.8	Problems

UNIT-II: **Nonlinear wave shaping**

2.1	Diode Clippers, Transistor clippers
2.2	clipping at Two independent levels
2.3	Comparators, applications of voltage comparators
2.4	Clamping operations, Clamping circuit taking source, diode resistance into account
2.5	Clamping circuit theorem
2.6	Practical Clamping Circuits
2.7	Effect of Diode characteristic on Clamping Voltage
2.8	Synchronized clamping

UNIT-III: Switching Characteristics of Devices

3.1	Diode as switch
3.2	piecewise Linear Diode characteristics
3.3	Diode switching Times , Transistor as a switch
3.4	Breakdown voltages , Transistor in Saturation
3.5	temperature variation of saturation parameters
3.6	Transistor switching times
3.7	Silicon controlled switch

UNIT-IV: Multi vibrators, Time base generators

4.1	Analysis and Design Astable Multivibrator
4.2	Analysis and Design Bitable Multivibrator
4.3	Analysis and Design Monostable Multivibrator
4.4	Analysis and Design of Schmitt trigger using transistor
4.5	General feature of Time base signal
4.6	Methods of generating time base wave form
4.7	Boot strap sweep generator
4.8	Transistor Miller time base generator
4.9	Transistor current time base generator
4.10	Methods of linearity improvement

13.2 ADD ON COURSE MATERIAL

14. MID QUESTION PAPERS

14.1 MID QUESTION PAPERS WITH KEY

14.2 SAMPLE ANSWER SCRIPTS

15. UNIT TEST QUESTION PAPERS WITH KEY

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15.1 SAMPLE UNIT TEST PAPERS

16. ASSIGNMENT QUESTIONS

16.1 SAMPLE ASSINGMENT SHEETS

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1.1 VISION OF INSTITUTION

To be a pioneer institute and leader in engineering education whose primary concern would be the development of the human race and betterment of society through their knowledge, technological understanding and the spirit of progress.

1.2 MISSION OF INSTITUTION

To create a conductive environment for student centric learning and industry institute interaction.

To integrate the state of the art infrastructure, facilities and cutting edge academic delivery.

To develop and nurture socially conscious technocrats through continuing education and research.

QUALITY POLICY

We at Siddhartha Institute of Engineering & Technology endeavor to uphold excellence in all aspects by adopting best practices in effort and effect.

1.3 VISION OF DEPARTMENT

To provide valuable resources for industry and society through excellence in technical education and research .

1.4 MISSION OF DEPARTMENT

To educate the students with the state of art technologies to meet growing challenges of the industry.

To carry out research through constant interaction with research organization and industry.

To equip the students with strong foundations to enable them for continuing education.

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2.1 PROGRAM EDUCATIONAL OBJECTIVES (PEO's):-

PEO1: To develop graduates with good technical knowledge and aspiration towards higher studies and research.

PEO2: To prepare the student to succeed in industry / technical profession through meticulous education.

PEO3: To develop practical skills by providing hands-on experience to the students.

2.2 PROGRAM SPECIFIC OUTCOMES (PSO's):-

PSO1: Ability to design and implement projects in the field of Electronic Communication systems, Image Processing, VLSI, Embedded system etc.

PSO2: Students will be furnished with necessary soft skills, aptitude and technical skills to work in the software and hardware Industry.

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3.1 PROGRAM OUTCOMES (POs):

PO. No.	Description
PO 1	**Engineering Knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO 2	**problem Analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO 3	**Design / Development of Solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO 4	**Conduct Investigations of Complex Problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO 5	**Modern Tool Usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO 6	**The Engineer and Society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO 7	**Environment and Sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO 8	**Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO 9	**Individual and Team Work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

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PO 10	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO 11	**Project Management and Finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO 12	**Life-long Learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.
	3.2 Program Specific Outcomes
PSO 1	Ability to design and implement projects in the field of Electronic Communication systems, Image Processing, VLSI, Embedded system etc.
PSO 2	Students will be furnished with necessary soft skills, aptitude and technical skills to work in the software and hardware Industry.

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	4 . ACADEMIC CALENDER FOR THE ACADEMIC YEAR 2018 – 2019	Rev.00

I SEM

S. No	EVENT	DATE	Duration
1.	Commencement of Instruction	9th July 2018	-------
2.	First Mid Term Examinations	4th to 6th Sept. 2018	-------
3.	Submission of First Mid Term Exam Marks to University on or before	15th Sept. 2018	-------
4.	Parent-Teacher Meeting	13' Oct. 2018	
5.	Dussehra recess	15' to 20th Oct. 2018	1 week
6.	Last date of Instruction	10th Nov. 2018	16 weeks
7.	Second Mid Term Examination	12th to 14th Nov. 2018	
8.	Preparation Holidays and Practical Examinations	15th to 24' Nov. 2018	1 week
9.	Submission of Second Mid Term Exam Marks to University on or before	24th Nov. 2018	-------
10.	End Semester / Supplementary Examinations	26th Nov. to 8th Dec. 2018	2 weeks
11.	Semester Break	10' to 15th Dec. 2018	1week

II SEM

S. No	EVENT	DATE	Duration
1	Commencement of Instruction	24th Dec. 2018	
2.	First Mid Term mid-1 Examinations	18th to 20' Feb. 2019	
3	Submission of First Mid Term Exam Marks to University on or before	27th Feb. 2019	
4	Parent-Teacher Meeting	9th March. 2019	
5.	Last date of Instruction	20th April 2019	16 weeks
6.	Second Mid Term Examinations	22nd to 24th April 2019	
7.	Preparation Holidays and Practical Examinations	25th to 5th may 2019	1 week
	Submission of Second Mid Term Examination to University on or before	2nd may 2019	
9.	End Semester / Supplementary Examinations	6th to18th May 2019	2 weeks
10.	Summer Vacation	20th May to 13th July 2019	8 weeks

DIRECTOR
ACADEMIC & PLANNING JNTUH

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	SIDDHARTHA INSTITUTE OF ENGINEERING AND TECHNOLOGY Vinoba Nagar, Ibrahimpatnam, R.R Dist.	SIET/ACA/F-01 Rev.00
	5. TIME TABLE FOR PDC FOR THE ACADEMIC YEAR 2018 – 2019	

Branch/Year: II-II

SUB: PULSE AND DIGITAL CIRCUITS

Day/period	1	2	3	4	12.30pm-1.10pm	5	6	7
TIME	9.00 am-10.00am	10.00am-10.50am	10.50am-11.40pm	11.40pm-12.30pm		1.10pm - 2.00pm	2.00pm - 2.50pm	2.50pm - 3.40pm
MON		PDC-A		PDC-B		PDC-B		
TUE		PDC-A		PDC-B				
WED	PDC-B							
THU	PDC-A							
FRI		PDC-A		PDC-B				
SAT		PDC-A						

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EC402ES: PULSE AND DIGITAL CIRCUITS
B.Tech. II Year II Sem.

L T P C
4 0 0 4

Course Objectives:

To explain the complete response of R-C and R-L-C transient circuits.

To explain clippers, clampers, switching characteristics of transistors and sampling gates.

To construct various multivibrators using transistors, design of sweep circuits and Sampling gates.

To discuss and realize logic gates using diodes and transistors.

Course Outcomes: At the end of the course, the student will be able to:

Understand the applications of diode as integrator, differentiator, clippers, and clamper Circuits.

Learn various switching devices such as diode, transistor, SCR. Difference between logic gates and sampling gates

Design multivibrators for various applications, synchronization techniques and sweep Circuits.

Realizing logic gates using diodes and transistors.

Understanding of time and frequency domain aspects.

Importance of clock pulse and its generating techniques.

UNIT - I

Linear Wave Shaping: High pass and low pass RC circuits and their response for Sinusoidal, Step, Pulse, Square, & Ramp inputs, High pass RC network as Differentiator, Low pass RC circuit as an Integrator, Attenuators and its application as a CRO Probe, RL and RLC Circuits and their response for Step Input, Ringing Circuit.

UNIT - II

Non-Linear Wave Shaping: Diode clippers, Transistor clippers, Clipping at two independent levels, Comparators, Applications of Voltage comparators. Clamping Operation, Clamping circuit taking Source and Diode resistances into account, Clamping Circuit Theorem, Practical Clamping Circuits, Effect of Diode Characteristics on Clamping Voltage,

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Synchronized Clamping.

UNIT - III

Switching Characteristics of Devices: Diode as a Switch, Piecewise Linear Diode Characteristics, Diode Switching times, Transistor as a Switch, Break down voltages, Transistor in Saturation, Temperature variation of Saturation Parameters, Transistorswitching times, Silicon-controlled-switch circuits.

UNIT – IV

Multivibrators: Analysis and Design of Bistable, Monostable, Astable Multivibrators and Schmitt trigger using Transistors.

Time Base Generators: General features of a Time base Signal, Methods of Generating Time Base Waveform, Transistor Miller Time Base generator, Transistor Bootstrap Time Base Generator, Transistor Current Time Base Generators, Methods of Linearity improvement.

UNIT - V

Sampling Gates: Basic operating principles of Sampling Gates, Unidirectional and Bidirectional Sampling Gates, Four Diode Sampling Gate, Reduction of pedestal in Gate Circuits

Realization of Logic Gates Using Diodes & Transistors: AND, OR and NOT Gates using Diodes and Transistors, DCTL, RTL, DTL, TTL and CML Logic Families and its Comparison.

TEXT BOOKS:

1. Millman's Pulse, Digital and Switching Waveforms –J. Millman, H. Taub and Mothiki S. Prakash Rao, 2 Ed., 2008, McGraw Hill.

2. Pulse, Switching and Digital Circuits - David A. Bell, 5th edition 2015, OXFORD University Press

REFERENCE BOOKS:

1. Pulse and Digital Circuits -Venkata Rao K, Rama Sudha K, Manmadha rao G, Pearson, 2010

2. Pulse and Digital Circuits – A. Anand Kumar, 2005, PHI.

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	7. GENERAL OBJECTIVES, SPECIFIC OBJECTIVES FOR PDC IN THE ACADEMIC YEAR 2018 – 2019	Rev.00

Year & Branch: **II-II B.TECH. ECE-A &B**
Academic year: **2018-2019**
Name of the subject: **PULSE AND DIGITAL CIRCUITS**
Name of the Faculty: **T KRISHNARJUNA RAO**
Designation: **ASSOCIATE PROFESSOR**
Department: **ECE**

COURSE DESCRIPTION: When devices such as diodes, bipolar junction transistors (BJTs) and field-effect transistors (FETs) are used in amplifiers, oscillators, rectifiers and other such applications, these devices are used either as linear or nonlinear circuit elements, for which they have to be used in a limited range of the transfer characteristic (defines the relation between the input and the output). If the operation goes beyond the linear region of the transfer characteristic, unwanted frequencies called harmonics—integer multiples of the fundamental frequency appear in the output of the circuit.

7.1 GENERAL OBJECTIVES:

- To know the process of linear wave shaping for LOW pass, HIGH pass RC circuits
- To understand the clipping and clamping process
- Ability to know the diode, transistor switching characteristics.
- To understand the concepts SCR as a switch.
- To understand the design and analysis of multivibrators.
- To understand the process of generating time base signal
- To understand operation of Schmitt trigger.
- To understand the operation of sampling gates
- To know the process of design logic gates using diode, transistor

7.2 SPECIFIC OBJECTIVES

Unit 1: Linear Wave Shaping

To study about linear wave shaping circuits and Non-linear wave shaping circuits for different input signals.

To describe the application of a low pass circuit as an integrator.

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To understand the principles of working of uncompensated and compensated attenuators and the operation of the attenuator circuit in CRO probe.

To derive the response of high pass RC, RL and RLC circuits to different types of inputs like Sinusoidal, pulse, step, square, ramp and exponential inputs.

To describe the application of high pass circuit as Differentiator.

To understand the operation of the ringing circuit.

Unit 2: Non-linear Wave Shaping

To study the principle of operation of various series and shunt clipping circuits

To study about diode comparators and double differentiators as amplitude comparators and it's applications .

To study the principle of operation of various clamping circuits and verify the clamping circuit theorem.

To describe the effect of diode characteristics on the clamping voltage.

To describe synchronized clamping.

Unit 3: Switching characteristics of Devices:

To study the principle of operation of diodes and transistors as switches.

To study the temperature dependence of the transistor on various parameters.

To understand the use of transistor switch.

To study the principle of operation of switching circuits using SCS.

Unit 4: Multivibratos, TIME BASE GENERATORS

To study the principle of operation of the multivibrators.

To study the applications of multivibrators.

To realize the need for a commutating condenser in a monostable multivibrator and bitable multivibrator.

To know the principle of operation of Time base generators

Ability to know the principle of operation of Miller Time base

To study the principle of operation of Bootstrap Time base generator

Unit 5: Synchronization and frequency division

To know the working of unidirectional and bidirectional sampling gates and their variations
To understand the working of sampling gates using Diodes (two, four and) and transistors.
Realization of logic gates using Diodes and Transistors

To understand the principle of operation of basic logic gates like AND, OR and NOT gates
To implement these gates using Diodes and Transistors
To understand the various logic families like DCTL, RTL, DTL, TTL and CML and their comparison

Student Learning Outcomes

Unit 1: Linear Wave Shaping

After completing this unit, the students are able to

Design linear wave shaping circuits using linear elements like R C and L.
Derive the expressions and plot the response of low pass RC circuits to different types of inputs namely sinusoidal, step, pulse, square-wave, exponential and ramp.
Describe the application of a low pass circuit as an integrator.
Understand the principles of working of uncompensated and compensated attenuators and the operation of the attenuator circuit in CRO probe.
Derive the response of high pass RC and RL circuits to different types of inputs like Sinusoidal, pulse, step, square, ramp and exponential inputs.
Describe the application of high pass circuit as Differentiator.
Understand the operation of the ringing circuit.
Find the response of RL and RLC circuits to step input.

Unit 2: Non-linear Wave Shaping

After completing this unit, the students are able to

Design various series and shunt clipping circuits and their combinations.
Understand the principle of operation of two level emitter coupled transistor clippers and noise clippers
Describe simple diode comparators and double differentiators as amplitude comparators.
Explain the applications of comparators.
Design various clamping circuits and verify the clamping circuit theorem.
Derive the necessary relations to plot steady state output.

Describe the effect of diode characteristics on the clamping voltage.

Describe synchronized clamping.

State and derive the clamping circuit theorem

Unit 3: Switching characteristics of Devices

After completing this unit, the students are able to

Use diodes and transistors as switches.

Describe the effect of inter-electrode capacitances on switching times.

Describe the switching times of devices and derive the necessary relations.

Describe the temperature dependence of the transistor on various parameters.

Understand the use of transistor switch as latch.

Realize the use of transistor switches with inductive and capacitive loads.

Design switching circuits using SCS.

Unit 4: Multivibratos & Time Base Generators

After completing this unit, the students are able to

Explain the principle of operation of the multivibrators.

Analyze and design Bistable, Monostable and Astable multivibrators and able to calculate and frequency / pulse width of the generated signal.

Plot the waveforms at various points in the circuit.

Describe the emitter coupled astable multivibrators

Use an astable multivibrator for applications such as voltage to frequency converter and frequency modulator

Understand the working of emitter coupled monostable multivibrator

Realize the need for a commutating condenser in a monostable multivibrator and bistable multivibrator.

Realize the application of a monostable multivibrator as a voltage to time converter

Analyze fixed bias and self bias bistable multivibrators

Analyze and design emitter coupled bistable multivibrator, also called Schmitt trigger

Describe the applications of bistable multivibrator circuits.

Able to design different types of Time base generators

Explain the features of the Time base signal.

Design Miller Time base Generator and explain the principle of operation.

Design Bootstrap Time base generator and explain the principle of operation.

Unit 5: Sampling gates and Realization of Gates using Diode & Transistor:

Understand the working of unidirectional and bidirectional sampling gates and their variations

Design sampling gates using Diodes (two, four and six) and transistors.

Describe the output by adjusting the levels of the control signal

Realize the applications of sampling gates in sampling scope

Derive a choppers stabilized amplifier using sampling gates

After completing this unit, the students are able to

Understand the principle of operation of basic logic gates like AND, OR and NOT gates

Implement these gates using Diodes and Transistors

Understand the various logic families like DCTL, RTL, DTL, TTL and CML and their comparison

Able to implement simple Boolean functions using different logic families.

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Ranga Reddy District-501 506.

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	8. COURSE OTCOMES FOR PDC IN THE ACADEMIC YEAR 2018 – 2019	Rev.00

Course Outcomes:

- Ability to know the applications of diode as integrator, differentiator, clippers, clamper Circuits.
- To Learn various switching devices such as diode, transistor, SCR.
- To know the Difference between logic gates and sampling gates
- Design multivibrators for various applications, synchronization techniques and sweep circuits.
- Realizing logic gates using diodes and transistors. Sampling gates

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	9. CO AND PO MAPING FOR PDC FOR THE ACADEMIC YEAR 2018 – 2019	Rev.00

9.1 Relationship of Course Outcomes to Program Outcomes

Course Name: PULSE AND DIGITAL CIRCUITS for Academic Year 2018-19 (II-II)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1.EC402ES	3	3	2	2	3	1	1	-	-	2	2	3
CO2.EC402ES	3	2	2	3	3	2	2	-	-	2	2	3
CO3.EC402ES	3	2	3	2	2	1	1	-	-	1	2	3
CO4.EC402ES	3	3	3	3	3	1	2	-	-	2	2	3
CO5.EC402ES	3	3	3	3	2	2	2	-	-	2	2	3
Average	3	2.6	2.6	2.6	2.6	1.4	1.6	-	-	1.8	2	3

9.2 Relationship of Course Outcomes to Program Specific Outcomes:

Course Name : PULSE AND DIGITAL CIRCUITS 2018-19 (II-II)

CO	PSO1	PSO2
CO1.EC402ES	3	2
CO2.EC402ES	3	2
CO3.EC402ES	3	2
CO4.EC402ES	3	2
CO5.EC402ES	3	2
Average	**3**	**2**

Faculty In-charge **HOD/Dept. of ECE.**

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	10. COURSE PLAN FOR PDC FOR THE ACADEMIC YEAR 2018 – 2019	Rev.00

Year & Branch: **II-II B.TECH. ECE-A &B**
Academic year: **2018-2019**
Name of the subject: **PULSE AND DIGITAL CIRCUITS**
Name of the Faculty: **T KRISHNARJUNA RAO**
Designation: **ASSOCIATE PROFESSOR**
Department: **ECE**

TEXT BOOKS:

1. Millman's Pulse, Digital and Switching Waveforms –J. Millman, H. Taub and Mothiki S. Prakash Rao, 2 Ed., 2008, McGraw Hill.
2. Pulse, Switching and Digital Circuits - David A. Bell, 5th edition 2015, OXFORD University Press
3. Pulse and Digital Circuits by MOTHIKI S. PRAKASH RAO.

REFERENCE BOOKS:

1. Pulse and Digital Circuits -Venkata Rao K, Rama Sudha K, Manmadha rao G, Pearson, 2010
2. Pulse and Digital Circuits – A. Anand Kumar, 2005, PHI.
3. Pulse and Digital Circuits by Yoganarasimha

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Institute of Engineering & Technology,
Vinobha Nagar(V), Ibrahimpatnam(M),
Ranga Reddy District-501 506.

Unit No.	Topic to be covered	T-BOOK R-BOOK	PROPOSED no.0f periods	PROPOSED DATE
1	**Linear wave shaping**		14	
1.1	High pass circuit, sinusoidal response	R-3	2	24-27.12.2018
1.2	Step and square and ramp response	R-3	2	28-29.12.18
1.3	Low pass ,sinusoidal and step response	R-3	2	31.12.18,02.01.2019
1.4	Square and Ramp response	R-3	1	3.01.19
1.5	RC Differentiator, Integrator	R-3	2	4-5.01.19
1.6	Attenuators and its applications as a CRO probe	R-3	1	7.01.19
1.7	RL and RLC Circuits and their Response for Step, Ringing Circuit	R-3	2	8-9.01.19
1.8	Problems	R-3	2	10-11.01.19
2.	**Nonlinear wave shaping**		12	
2.1	Diode Clippers, Transistor clippers	R-2	3	17-19.01.19
2.2	clipping at Two independent levels	R-2	1	21.01.19
2.3	Comparators, applications of voltage comparators	R-2	1	22.01.19
2.4	Clamping operations, Clamping circuit taking source, diode resistance into account	R-2	2	23-24.01.19
2.5	Clamping circuit theorem	R-2	1	25.01.19
2.6	Practical Clamping Circuits	R-2	2	28-29.01.19
2.7	Effect of Diode characteristic on Clamping Voltage	R-2	1	30.01.19
2.8	Synchronized clamping	R-2	1	31.01.19

PRINCIPAL
SIDDHARTHA
Institute of Engineering & Technology,
Vinobha Nagar(V), Ibrahimpatnam(M),
Ranga Reddy District-501 506.

Unit No.	Topic to be covered			
3	**Switching Characteristics of Devices**		8	
3.1	Diode as switch	T-3	1	01.02.19
3.2	piecewise Linear Diode characteristics	T-1	1	02.02.19
3.3	Diode switching Times , Transistor as a switch	T-3	2	4-5.02.19
3.4	Breakdown voltages , Transistor in Saturation	T-3	1	6.02.19
3.5	temperature variation of saturation parameters	T-3	1	07.02.19
3.6	Transistor switching times	T-3	1	08.02.19
3.7	Silicon controlled switch	T-3	1	11.02.19
4	**Multi vibrators, Time base generators**		19	
4.1	Analysis and Design Astable Multivibrator	R-3	2	12-13.02.19
4.2	Analysis and Design Bitable Multivibrator	R-3	2	14-15.02.19
4.3	Analysis and Design Monostable Multivibrator	R-3	2	16-22.02.19
4.4	Analysis and Design of Schmitt trigger using transistor	R-3	2	23.02.19
4.5	General feature of Time base signal	R-3	2	26.0219
4.6	Methods of generating time base wave form	R-3	2	28.02.19
4.7	Boot strap sweep generator	R-3	2	01.03.19
4.8	Transistor Miller time base generator	R-3	2	02.03.19
4.9	Transistor current time base generator	R-3	1	5.03.19
4.10	Methods of linearity improvement	R-3	2	6.3.19
5	**Sampling gates, Realization of logic gates Using Diodes and Transistors**		13	
5.1	Basic operating principles of sampling gates	R-2	1	7.3.19
5.2	Unidirectional and bidirectional sampling gates	R-2	2	8-11.3.19
5.3	Four diode sampling gates	R-2	1	12.319
5.4	Reduction of pedestal in Gate Circuits	R-2	2	13-14.3.19
5.5	AND, OR and NOT gates using Diodes & Resistor	R-2	3	15-19.3.19
5.6	DCTL,RTL,DTL Logic familys	R-2	2	22-23.3.19
5.7	TTL, CML logic families and comparison	R-2	2	25-26.319

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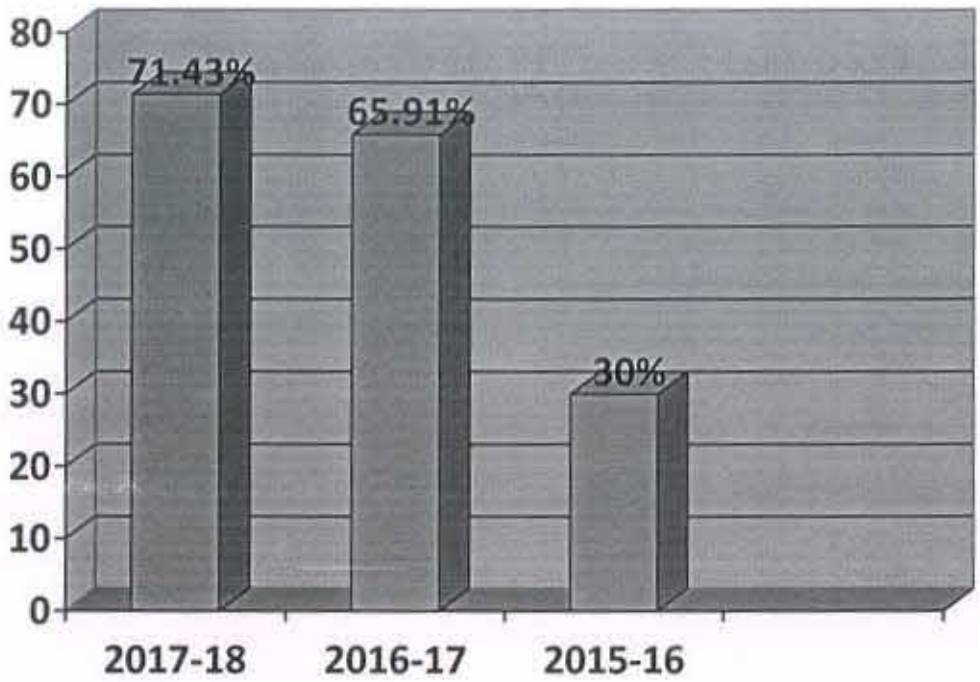
PASS PERCENTAGE:



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	12. QUESTION BANK	Rev.00

12.1 SHORT QUESTIONS

UNIT-I : Linear Wave Shaping

1. Obtain the response of high pass RC circuit for a ramp input – 3 M
2. Define % tilt of RC circuit. – 2 M
3. Define rise time. – 2 M
4. Draw and briefly explain the RC differentiator circuit – 3 M
5. Derive an expression for the output of a high-pass circuit excited by a ramp input. – 3 M
6. What do you mean by linear network? – 2 M
7. Why RC circuits are commonly used compared to RL circuits. – 2 M

Unit 2: Non-linear Wave Shaping

1. Write the applications of voltage comparator. – 2
2. Draw Negative biased Negative clipper circuit. – 3
3. What is meant by clipping in wave shaping? – 2
4. Explain Clipping at two independent levels with circuit – 3
5. Draw the basic circuit diagram of negative peak clamper circuit. – 3
6. Distinguish between comparators and clipping circuits – 2

Unit 3: Switching characteristics of Devices

1. Draw the piecewise linear diode characteristics. – 3
2. When transistor acts as a switch? – 2
3. Explain the variation of saturation parameters of transistor with temperature? – 2
4. How does diode acts as a switch? – 2
5. What do you mean by turn ON time of a transistor? – 3

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Unit 4: Multivibratos & Time Base Generators

1. Define multivibrator. – 2
2. Compare different multivibrators. – 2
3. Write a basic principle of time base generator. – 2
4. Write the Methods of Generating Time Base Waveform. – 3
5. Write the difference between current time base generator and voltage time base Generators – 3
6. List different switching times of a diode. – 2
7 Explain how diode acts as a switch. – 3

Unit 5: Sampling gates and Realization of Gates using Diode & Transistor:

1. Explain the frequency division in the sweep circuit. – 3
2. Define positive and negative logic systems. – 3
3. List out the applications of sweep circuits. – 2
4. Draw the diagram of OR gate using diodes. – 2
5. Why totem pole is used in DTL. – 3
6. How do sampling gates differ from logic gates? – 3
7. Compare MOS and CMOS families – 2

12.2 LONG QUESTION

UNIT-I : Linear Wave Shaping

1. Draw the output of the low pass RC circuit for different time constant to
   a) Pulse input. 5M
   b) Step voltage input 5M
2. Prove that for any periodic input waveform the average level of the steady state Output signal from RC high pass circuit is always zero. 5M
   b) Draw and explain the response of RLC circuit for step input. 5M
3. A symmetrical square wave whose peak-to-peak amplitude is 8V and whose average Value is zero is applied to an RC integrating circuit. The time constant is equal to Half -period of the square wave. Find the peak to peak value of the output amplitude 10 M

4.Explain the working of high-pass RC circuit as a differentiator. 5M

5.Derive the expression for rise time of integrating circuit and prove that it is Proportional to time constant and inversely proportional to upper 3 dB frequency. 10M

Unit 2: Non-linear Wave Shaping

1. Classify different types of clipper circuits. Draw their circuits and explain their Operation and also transfer characteristics? 5M
2. State and prove clamping circuit theorem. 5 M
   Explain negative peak clipper with and without reference voltage. 5M
3. What is meant by comparator? Explain the applications of voltage comp 5M

Unit 3: Switching characteristics of Devices

1. Discuss in detail about breakdown voltages of a transistor 5M
2. List out and derive the different Temperature variation of Saturation Parameters of a transistor 5M
3. a)Design Transistor switch circuit. 5M
   b) Explain in detail about the Silicon-controlled-switch circuits. 5M
4. List and define all the transistor switching times, with a neat diagrams 5M

Unit 4: Multivibratos & Time Base Generators

1. Explain with neat diagram the following methods of liberalizing a voltage sweep.
   a) Miller Sweep 5M
   b) Bootstrap weep. 5M
2. Draw and explain the working principle of bitable multivibrator circuit and also Explain the merits and limitations of it. 5M
3. Draw the circuit of a lincar current sweep and explain its operation with wave forms. Explain the necessity of generating trapezoidal wave form. 5M
4. With the help of neat circuit diagram and waveform, explain the principle of operation of collector coupled monostable multivibrator 5M
5. With the help of a neat circuit diagram and waveforms, explain the working of a transistor bootstrap time base generator. 5M
6. Draw the circuit diagram of Transistor Miller Time Base generator and explain its operation 5M

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Unit 5: Sampling gates and Realization of Gates using Diode & Transistor:

1. a)Explain the operation of linear bidirectional sampling gate using transistors. 5M
   b) Explain in detail the junction diode switching times. 5M

2. a)Explain about basic operation principles of sampling gates. 5M
   b) Write the advantages and disadvantages of unidirectional diode gate. 5M

3. Draw and explain 2-input NAND gate with functional table. 5M

4. List out the few comparisons of TTL, RTL and CML logic families 5M

5. a)Compare DTL and TTL families 5M

   b) Discuss about RTL logic family in detail, with one example. 5M

6.a)Realize AND gate and OR gate using diodes. 5M
   b) Explain about Transistor – Transistor logic. Also mention the types of output configuration 5M

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Vinobhanagar, Ibrahimpatnam, R.R.District-501506

Name of the Exam: B.TECH II-IIMID-I TERM EXAMS FEB-2019

Branch:ECE Subject: PDC

Date:19-02-19-AN Time:1.00Hr

Answer any two questions from the following (all questions carry equal 5 Marks) Max.Marks:10 M

1. Draw and explain the output wave forms of low pass RC circuits for pulse input, step input?

2. Explain the operation of High pass RC circuit for square wave input signal?

3. Classify different types of clippers? Explain their operation?

4. What is clamper explain Biased clamper?

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Vinobhanagar, Ibrahimpatnam, R.R.District-501506

Name of the Exam: B.TECH II-IIMID-I TERM EXAMS FEB-2019

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II B.Tech. II Sem., Ist Mid-Term Examinations, February – 2019

Branch: ECE **Subject: PDC**

Date: 19-02-19-AN **Objective Exam** **Time: 20min**

Name: _____ **Hall Ticket No.** _____

Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 10.

I. Choose the correct alternative:

1. The waveform which preserves its form when transmitted through a linear network is a____. [A]

A) Sine wave B) Step signal C) impulse signal D) ramp signal

2. The rise time of the output of a low pass RC circuit is given by [A]

A) 2.2 RC B) 0.35/fH C) 2.2τ D) all the above

3. What is the name of the circuit which converts square wave in to spikes [C]

A) Low pass RC B) Bi stable multi C) High pass RC D) Monoshot

4. When RC high pass circuit act as a differentiator? [A]

A) RC<<T B) RC>>T C) RC=T D) RC=0

5. A circuit that adds positive or negative dc voltage to an input sine wave is called [A]

A) Clamper B) clipper C) diode clamp D) limiter

6. A clamping circuit is also called as _____. [C]

A) Dc restorer B) dc reinserted C) both A and B D) none of the above

7. The upper cut-off frequency of a low pass RC circuit is _____. [B]

A) Zero B) $1/2\pi RC$ C) ∞ D) none of the above

8. What is the response of step input to a high pass RC circuit [C]

A) V e-t/RC B) V (1- et/RC) C) V et/RC D) V (1- e-t/RC)

9. A transistor acts as an amplifier when it is in [C]

A) Saturation region B) Cut-off region C) Active region D) none of the above

10. CRO Probe working as _____ [C]

A) Integrator B) Differentiator C) Attenuator D) none

II. Fill in the Blanks:

11. For DC input signal capacitor C acts as Short Circuit
12. The average value of the output value of an RC high pass circuit is 0.
13. Time constant of RL circuit is $\frac{L}{R}$.
14. The clamping theorem is given by $\frac{A_f}{A} = \frac{R_f}{R}$.
15. A network comprising of linear elements is called Linear network.
16. In Series clamping a reference voltage source is connected in series with the diode.
17. In a positive Clipper, when the diode is OFF, the output follows the input.
18. A circuit which clamps the negative peak of a signal to zero level is called Negative clamper
19. Rise time is defined as the time by the voltage to rise from 0.1 to 0.9 of its final value.
20. Diode applications Rectifier, ON/OFF switch, Regulator.

-oOo-

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	BLOOMS TAXONOMY LEVEL FOR PDC MID-1 QUESTION PAPER	Rev.00

Q.NO	NAME OF THE QUESTION	BLOOMS TAXONOMY LEVEL
1	Draw and explain the output wave forms of low pass RC circuits for pulse input, step input? 5M	APPLY
2	Explain the operation of High pass RC circuit for square wave input signal? 5M	UNDESTAND
3	Classify different types of clippers? Explain their operation? 5M	REMEMBER
4	What is clamper explain Biased clamper? 5M	UNDERSTAND

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Name of the Exam: B.TECH II-IIMID-II TERM EXAMS APR-2019

Branch:ECE **Subject: PDC**

Date:23-04-19-AN **Time:1.30min**

Answer any two questions from the following (all questions carry equal 5 Marks) **Max.Marks:10 M**

1. Draw and explain the working principle of bitable multivibrator circuit and alsoexplain the merits and limitations of it.
2. Draw the circuit diagram of Transistor Miller Time Base generator and explain its operation
3. With the help of neat circuit diagram and waveform, explain the principle ofOperation of collector coupled monostable multivibrator
4. Realize AND gate and OR gate using diodes.

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Vinobhanagar, Ibrahimpatnam, R.R.District-501506

Name of the Exam: B.TECH II-IIMID-II TERM EXAMS APR-2019

Branch: ECE **Subject: PDC**

Date: 23-04-19-AN **Time: 1.30min**

Answer any two questions from the following (all questions carry equal 5 Marks) **Max.Marks:10 M**

1. Draw and explain the working principle of bitable multivibrator circuit and also explain the merits and limitations of it.
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II B.Tech. II Sem., IInd Mid-Term Examinations, April – 2019

Branch: ECE **Subject: PDC**

Date: 23-04-19-AN **Objective Exam Time: 30min**

Name: _____ **Hall Ticket No.** _____

Answer All Questions. All Questions Carry Equal Marks. Time: 30 Min. Marks: 10.

I. Choose the correct alternative:

1. Which of the following logic family has highest fan-out? (D)
A) ECL B) TTL C) DTL D) CMOS

2. A sinusoidal waveform can be converted to a square waveform by using _____ (C)
A) Astable multivibrator B) Bitable multivibrator C) Schmitt trigger D) None of the above

3. In Miller time base generator, which of the following is used (B)
A) An inverting amplifier with a gain of unity B) an inverting amplifier with a gain of infinity C) Non-inverting amplifier with a gain of unity D) non-inverting amplifier with a gain of infinity

4. Bootstrap's sweep circuit produces _____ type of waveform. (A)
A) Positive going Ramp B) negative going Ramp C) either A or B D) Both A and B

5. Circuit which consist of a quasi-stable state is called (B)
A) Bistable circuit B) nonstable circuit C) tri stable circuits D) tristate circuit

6. To get a saw-tooth output waveform, the restoration time is (A)
A) Zero B) rise time C) storage time D) infinity

7. Bootstrap's sweep circuit produces _____ type of waveform. (A)
A) Positive going Ramp B) negative going Ramp C) either A or B D) Both A and B

8. Applications of time base generator (C)
A) Multivibrator B) logic gates C) CRO D) A & B

9. Multivibrator has how many states? (C)
A) 0 B) 1 C) 2 D) 4

10. Transistor saturation region operation in the following biase (C)
A) R.B, R.B B) R.B, F.B C) F.B, F.B D) F.B, R.B

II. Fill in the Blanks

11. A Time Base generator is an electronic circuit which generates an output voltage or current waveform.

12. The No of quasi stable states of mono stable is 1

13. When the diode is forward biased it acts as ON Switch

14. The basic TTL gate is AND / NAND

15. Schmitt trigger is a Sine to Squarewave Converter

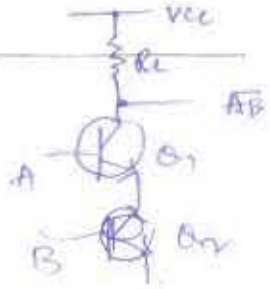
16. Which is the best logic family in bipolar technology TTL

17. Which logic gate having high fan-out CMOS

18. Define sampling gate An electronic Device which produces the replica of the out

19. Transistor saturation voltage in CE configuration 0 to 0.3 V

20. Draw any RTL logic gate



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	BLOOMS TAXONOMY LEVEL FOR PDC MID-2 QUESTION PAPER	Rev.00

Q.NO	NAME OF THE QUESTION	BLOOMS TAXONOMY LEVEL
1	Draw and explain the working principle of bitable multivibrator circuit and also Explain the merits and limitations of it? 5M	APPLY
2	Draw the circuit diagram of Transistor Miller Time Base generator and explain its operation?5M	APPLY
3	With the help of neat circuit diagram and waveform, explain the principle of operation of collector coupled monostable multivibrator?5M	UNDERSTAND
4	Realize AND gate and OR gate using diodes?-5M	APPLY

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II. B.Tech II sem R16 EXAMINATION - FEB 2019

YEAR/SEM: II - II

BRANCH: ECE

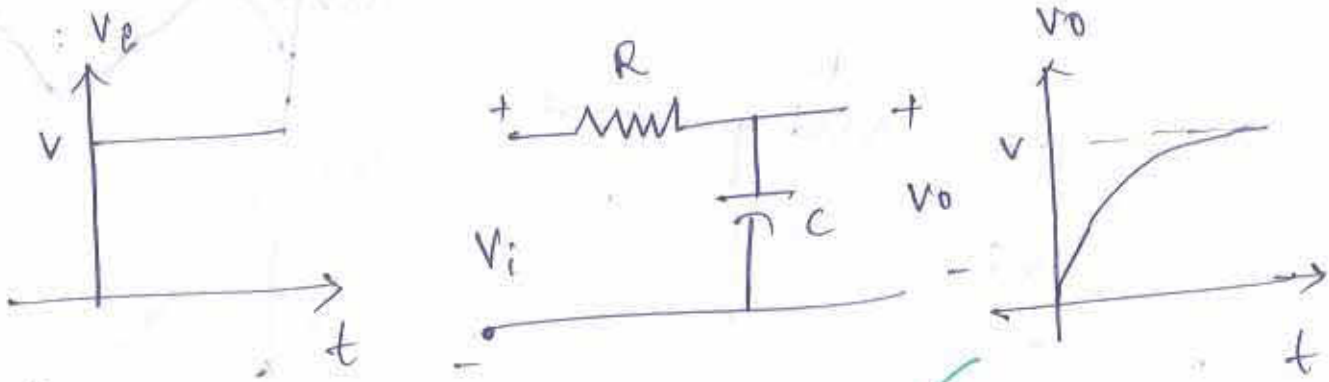
Date: 19.02.2019

SUB: PDE

Internal: 1

(7) Draw and Explain the output wave form of Low pass RC circuits for pulse, Step input

Low pass RC circuit allows only low frequency signals it attenuates high frequency signals. so the capacitor acting as open circuit for DC. and short circuit for AC. current. Resistor act as short ckt for DC current.

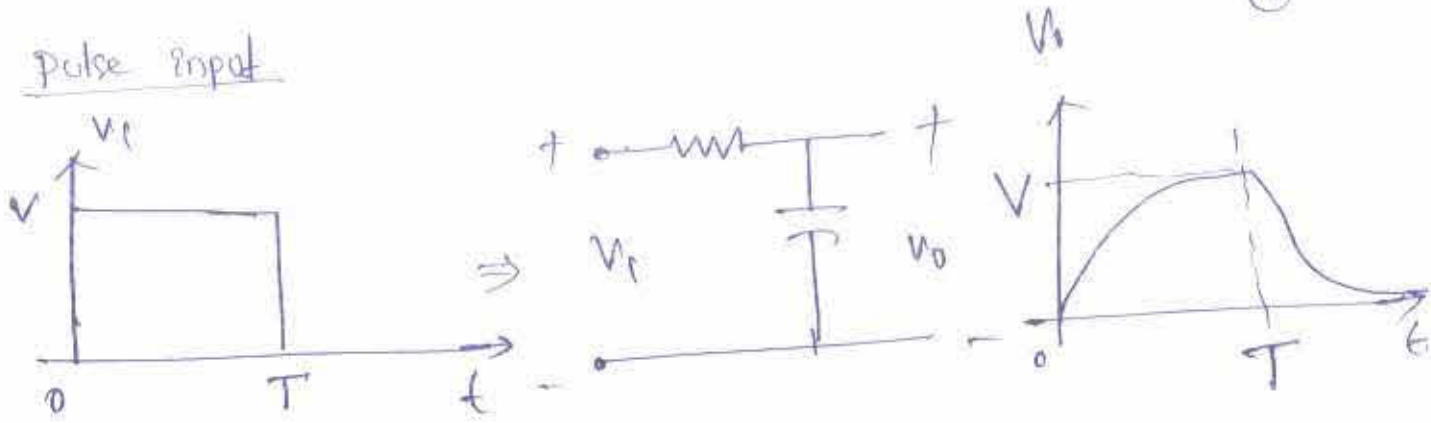


$V_i = V \quad t > 0$

$V_i = 0 \quad 0 \cdot w$

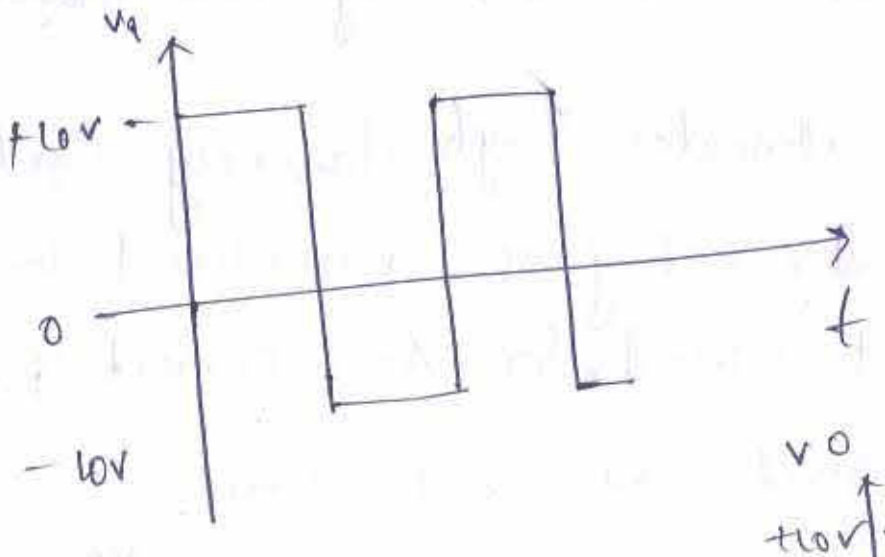
$V_o = v(1-t)e^{-t/RC}$

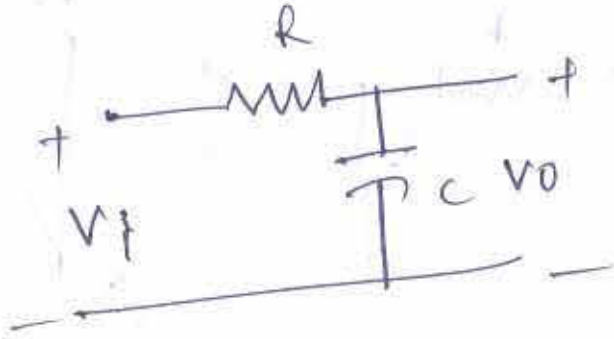
Pulse Input

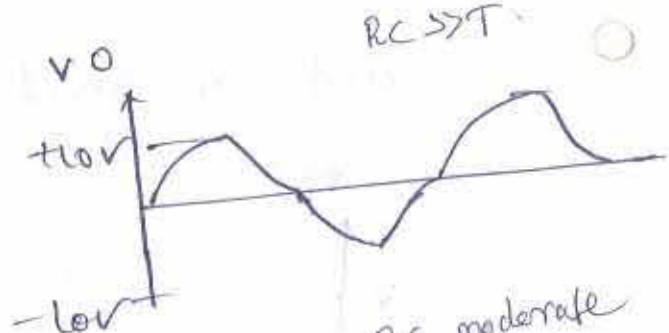


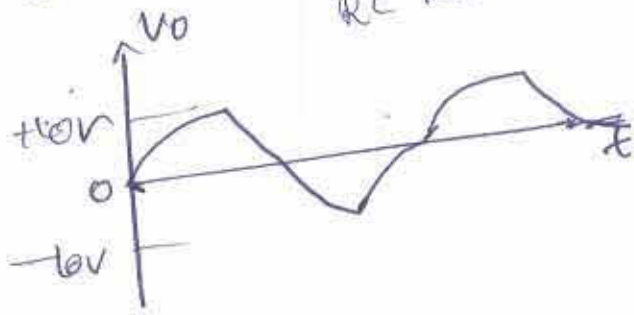
2. Operation of Highpass RC Circuit for Square wave Input Signal ?

Input Signal









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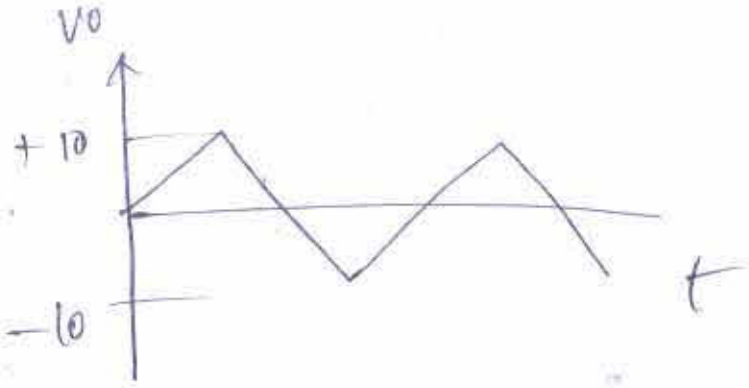

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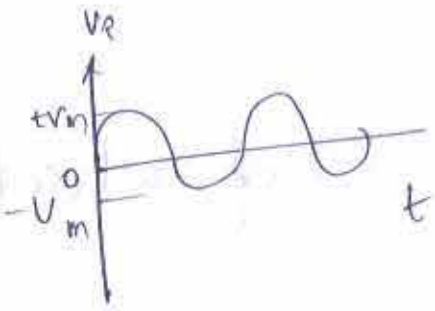
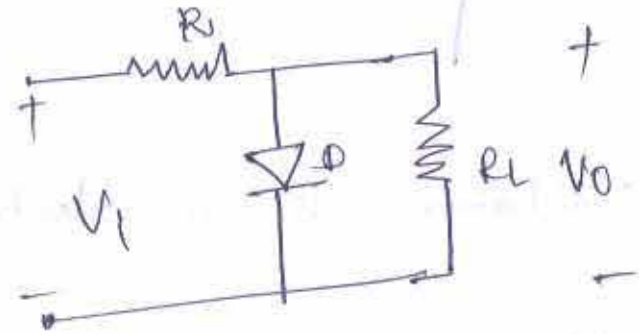
3. Types of Clippers:

① positive clipper ② Negative clipper

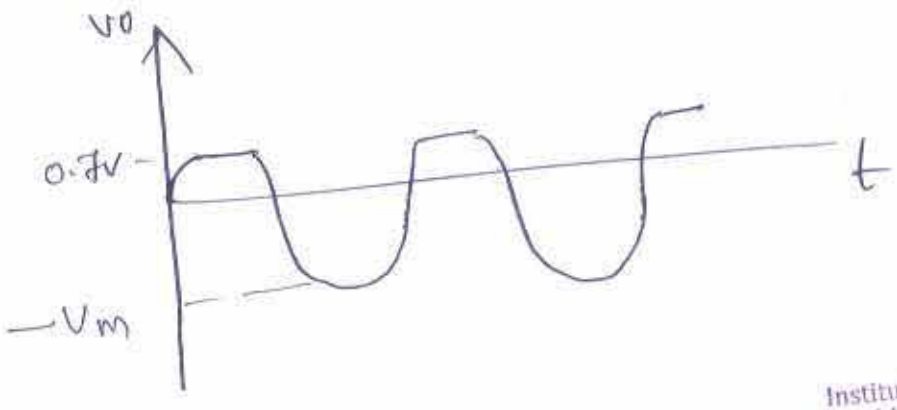
③ Biased clipper.

positive clipper (shunt clipper)





output waveform



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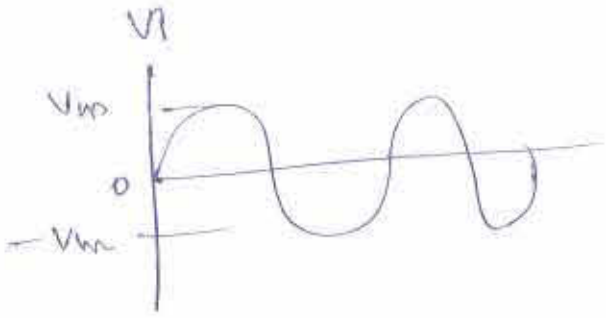
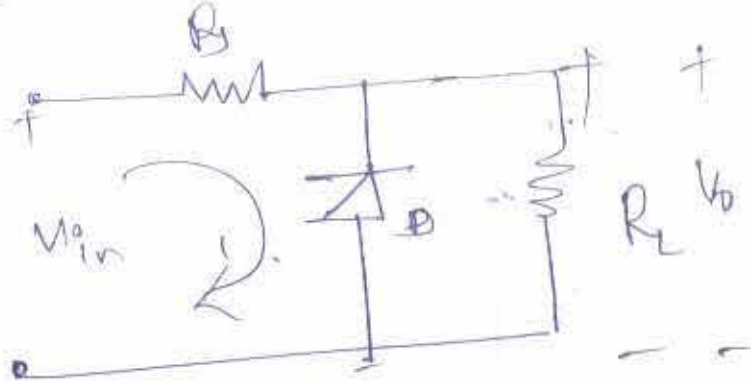
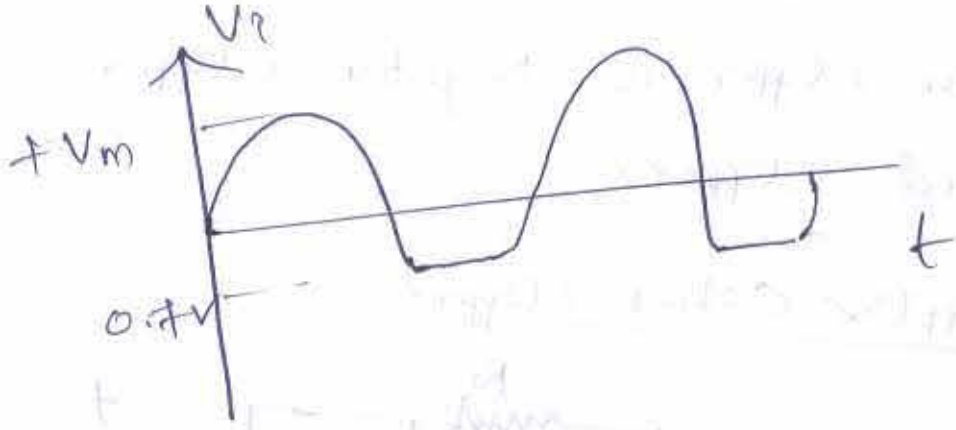
Negative Shunt clipper





Output waveform

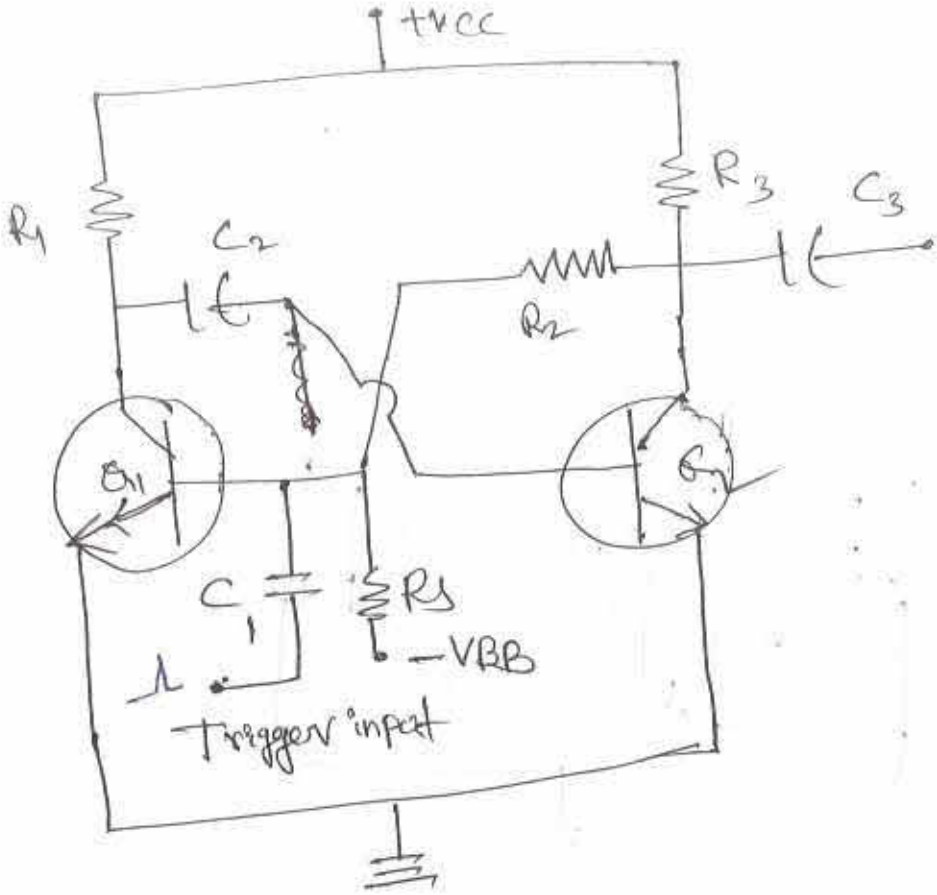


(4) Clamper is an electronic circuit which adds DC level to the input signal, Biased clamper adds more dc level to the given input signal

3.

Q. Design and Analyses of Monostable Multivibrator?

3



→ Monostable Multivibrator has one stable state, one unstable state.

→ Apply −VBB, +VCC, Q1 R.B C2 fully charge

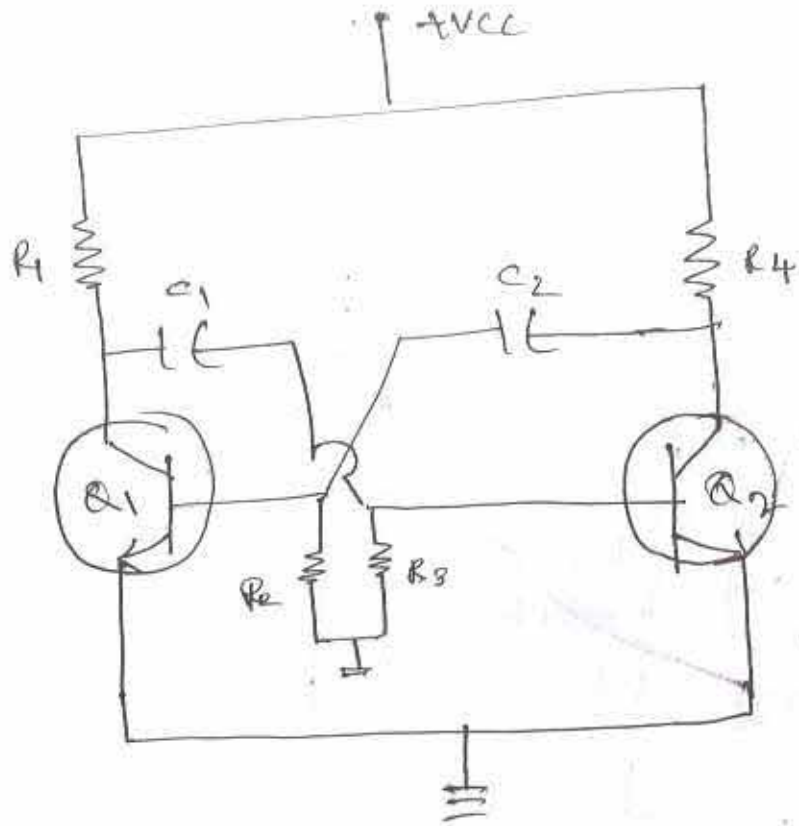
∴ C2 voltage given to Base of Q2 "ON"

So Vout is equal to Zero (Stable)

→ Then Apply +ve Trigger for Q1

C2 discharge Q2 R.B C2 is fully charging

Q. Design and Analysis of Astable Multivibrator?



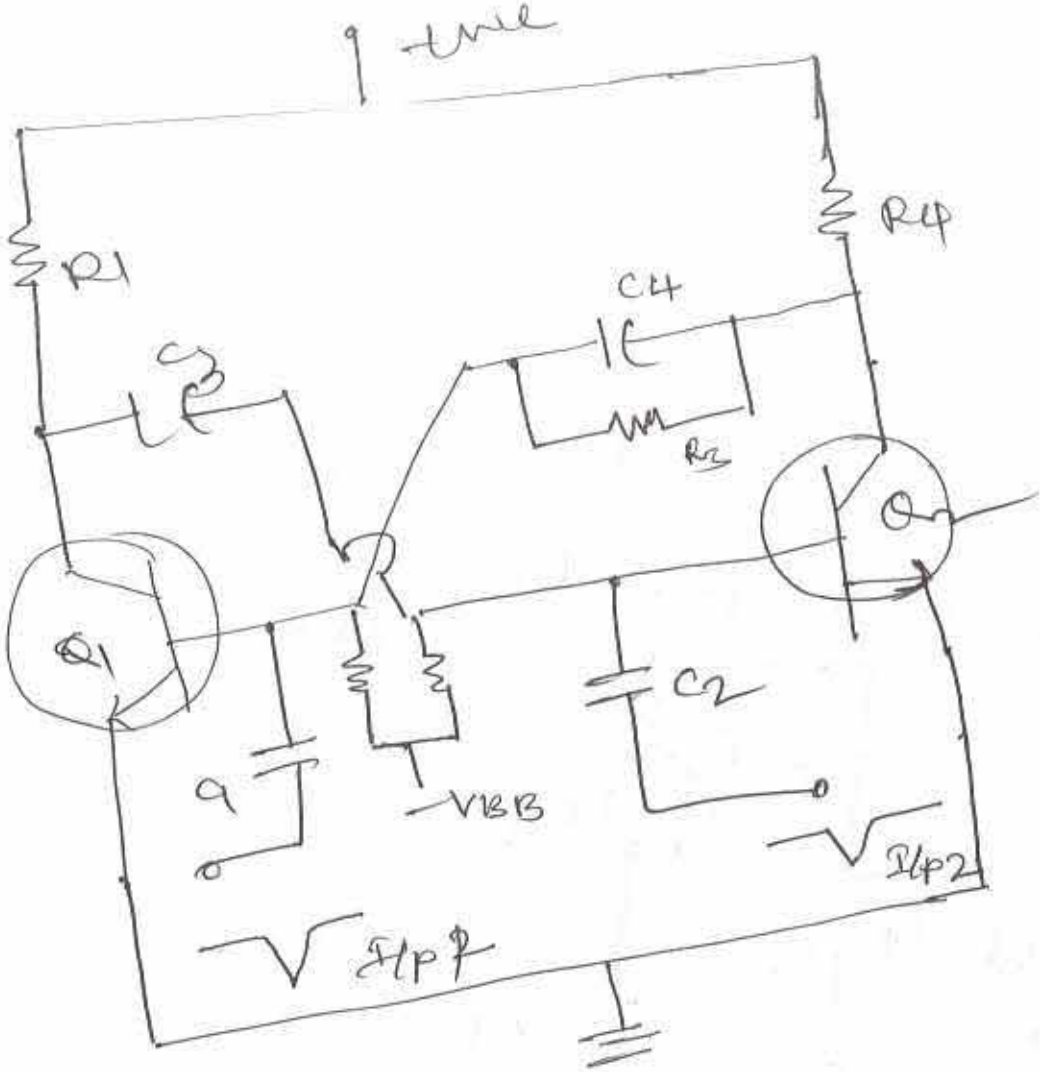
→ output voltage is Logic high Quasi Stable at high voltage

→ Then Trigger pulse goes to low Q_1 RB C_2 high, Q_2 turn ON Vout Low (Stable State).

SUB: PDC
Year: II-II

MID-2 Key
Academic year: 2018-19

1. Operation of Bistable multivibrator? and Merits and Limitations?



→ It is a two stable state device i.e stable at Q_1, Q_2

→ Apply $-V_{BB}$, $+V_{CC}$, Q_1, Q_2 Transistors in R.B so C_3, C_4 charging volt high

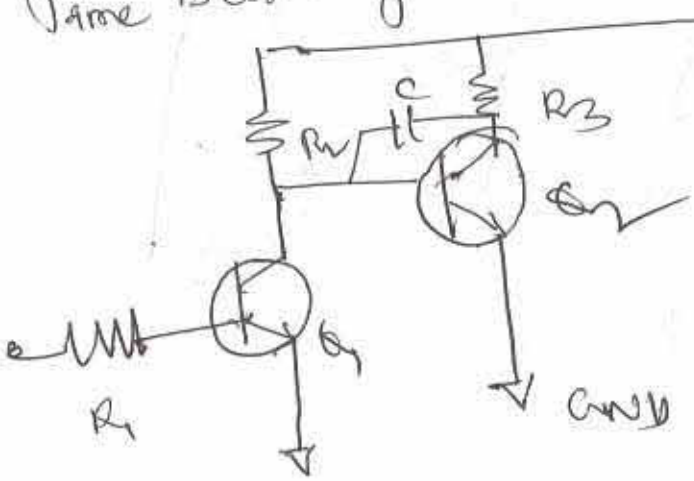
→ Apply Trigger input "i" Q_1 R.B C_3 high

Q_2 turn ON, C_4 is low (Stable at low)

⇒ Then Apply Tregeger input '2' Q_2 R.B C_4 high, Q_1 turn ON C_3 low, so Q_2 R.B C_4 high (Stable at high)

---

2. Draw Ein Circuit Diagram of Transistor Miller Time Base generator



→ The polarity of Sweep voltage is Negative

→ Inverting Amplifier is Used in this ckt

→ The open ckt gain of amplifier A = ∞

→ The Linearity is more

→ Source voltage is equal to VC

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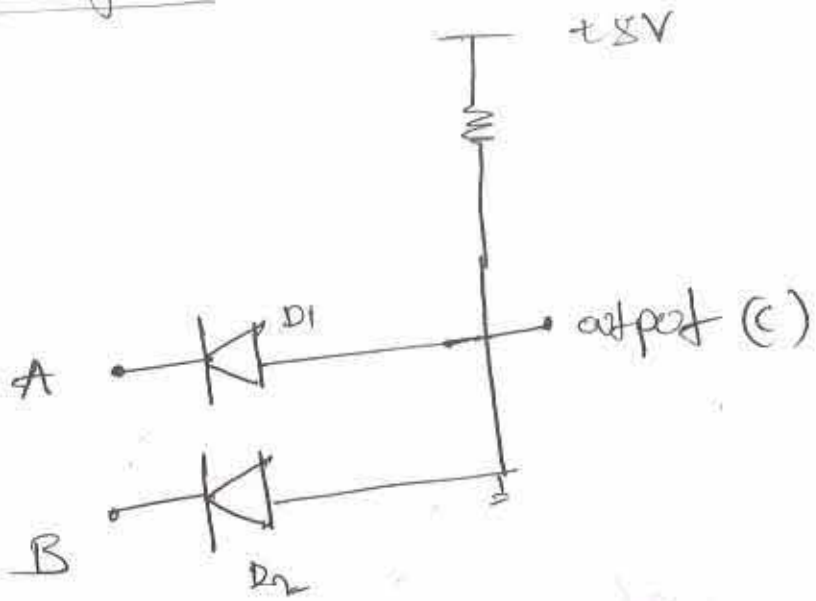
4. Realization of AND gate and OR gate using Diode?

AND gate



AND gate Truth table

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Boolean Expression

$C = A \cdot B$

1. A=0, B=0, Diode D1, D2 Both are Turn "ON" output voltage is Zero

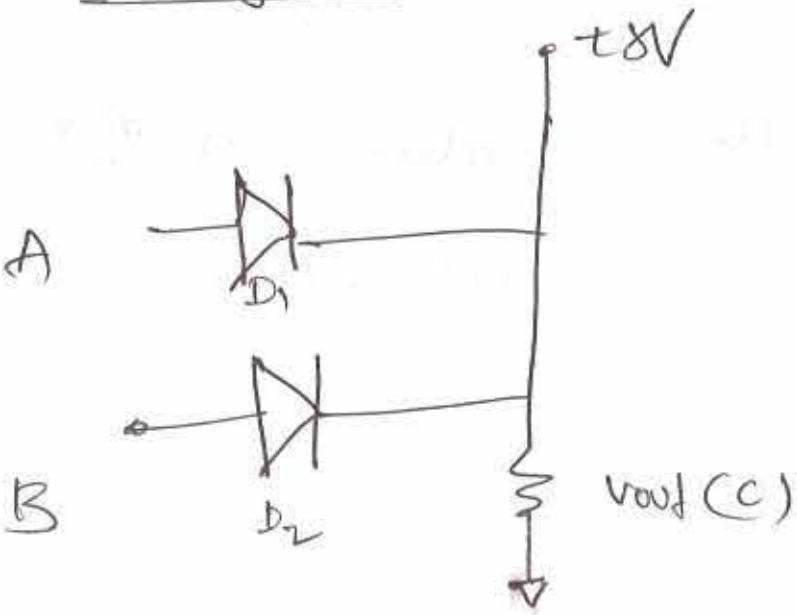
2. ~~A=0~~, B=1 Diode D1 "ON", D2 OFF output voltage is Zero.

3. A=1, B=0 Diode D_1 OFF, D_2 ON again output voltage is equal to Zero

4. A=1, B=1 Both Diodes are in Reverse Biase so output voltage is equal to 1

Logic 1

OR gate



T.T

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

Boolean Expression: $C = A + B$

1. A=0, B=0 D_1, D_2 acting as open ckt so output voltage is "0"

2. A=0, B=1, D_1 OFF. D_2 starts conducting. So Vout = high

3 A=1, B=0 D_2 OFF D_1 starts conducting

Vout = high

4. A=1, B=1 D_1, D_2 starts conducting

Vout = high.

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	ASSIGNMENT QUESTIONS FOR PDC	Rev.00

MID -1 ASSIGNMENT QUESTIONS

1. Draw the output of the low pass RC circuit for different time constant to pulse input and square input pulse ?
2. Classify different types of clipper circuits and explain their operation and also transfer Characteristics?
   - 2.a Positive Clipper ?
   - 2.b Negative clipper?
   - 2.c Positive clipper with positive bias and negative bias?
   - 2.d Negative clipper with Negative bias and positive bias?
3. Difference between high pass, low pass rc circuits for different input signals?

MID -2 ASSIGNMENT QUESTIONS

1. Explain in detailed about Silicon Diode controlled switch circuits?
2. Explain with neat Diagram for the time base Generator of Miller Sweep circuits?
3. Explain with neat Diagram for the time base Generator of Bootstrap circuits?
4. Draw and Explain the working principle of Bistable Multivibrator?
5. Explain the operation of unidirectional and Bi-directional Sampling gates?
6. Realize AND , OR Gate using Diode & Transistor?

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Vinobha Nagar(V), Ibrahimpatnam(M),
Ranga Reddy District-501 506.

G. Jayasri

17U91A04O4

pde Assignment-1

ECE-B

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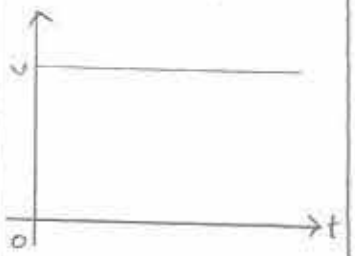
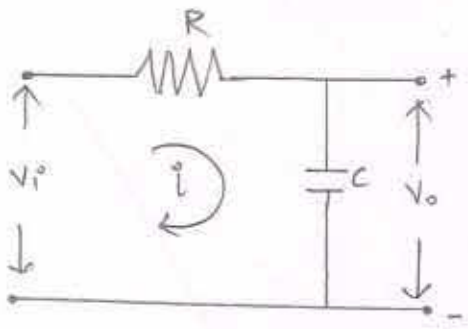
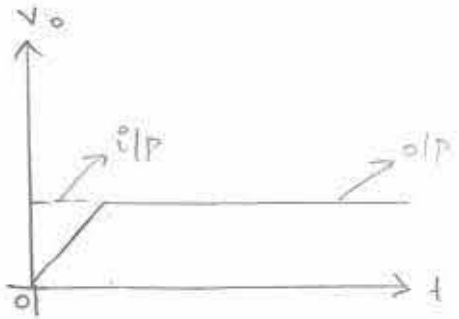
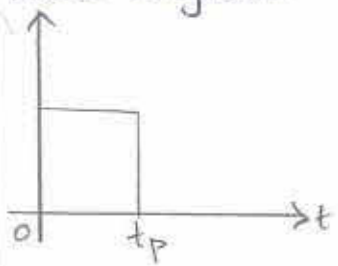
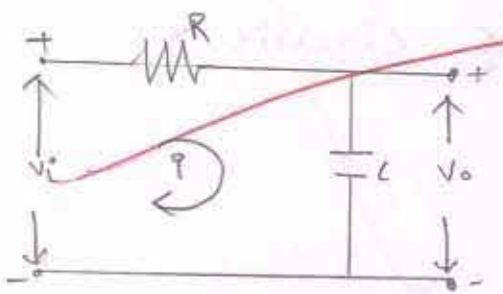
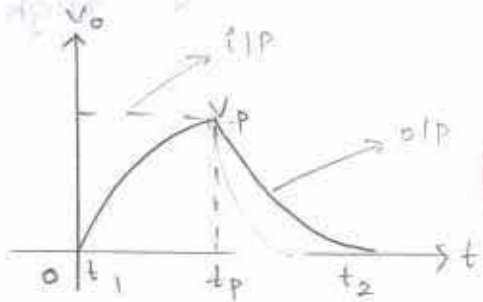
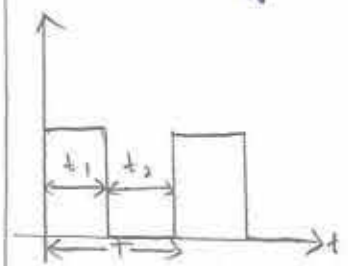
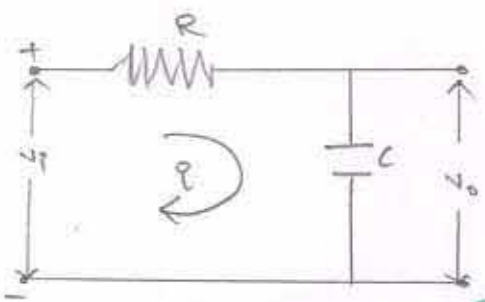
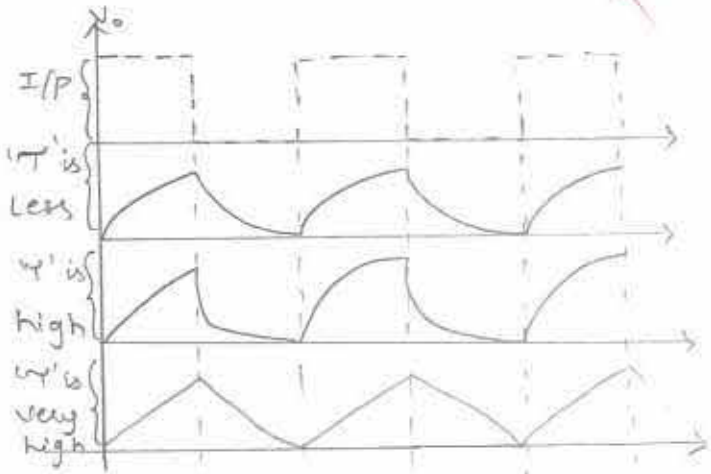
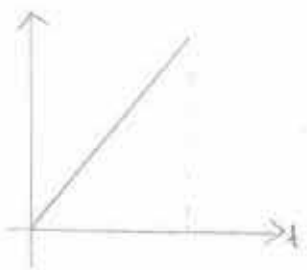
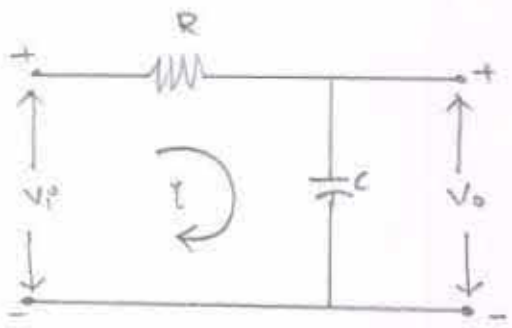
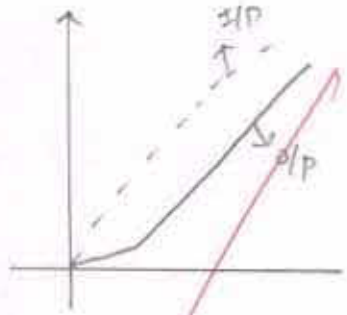
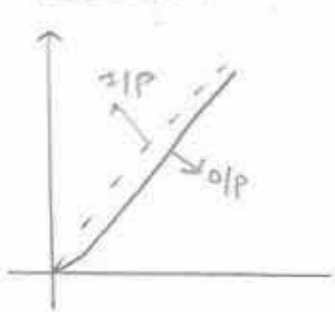
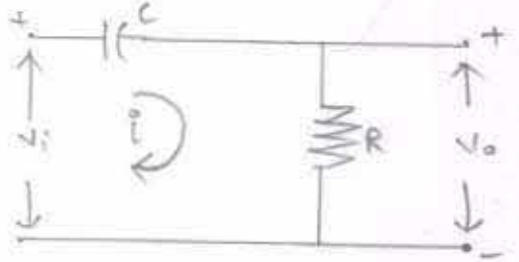
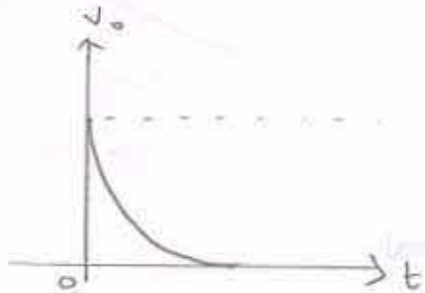
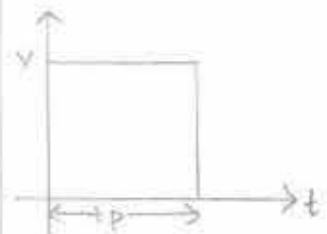
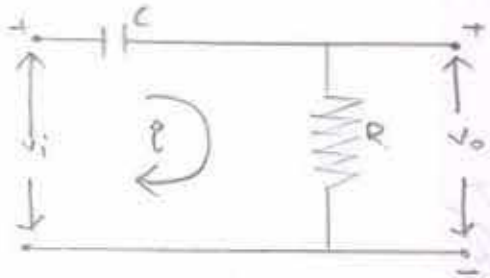
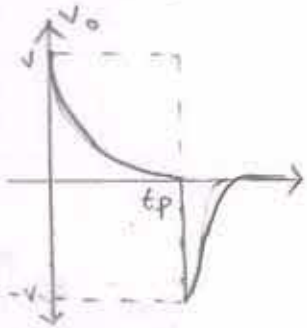
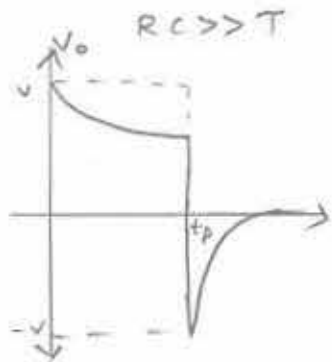
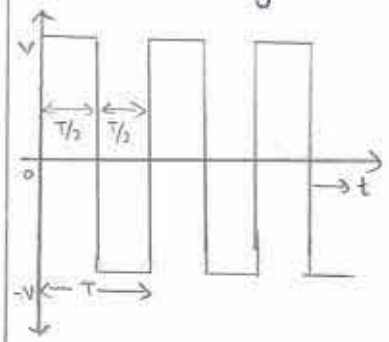
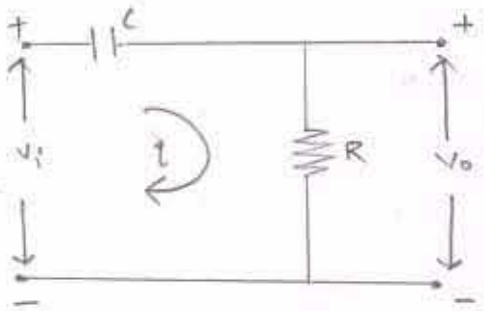
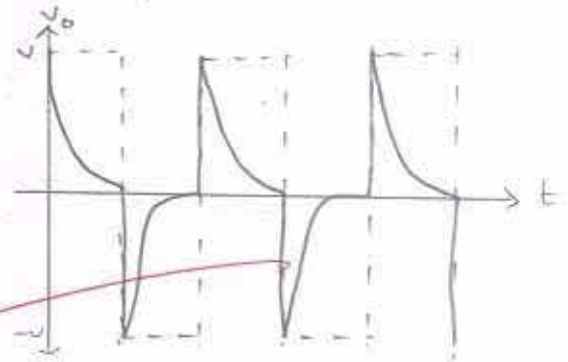
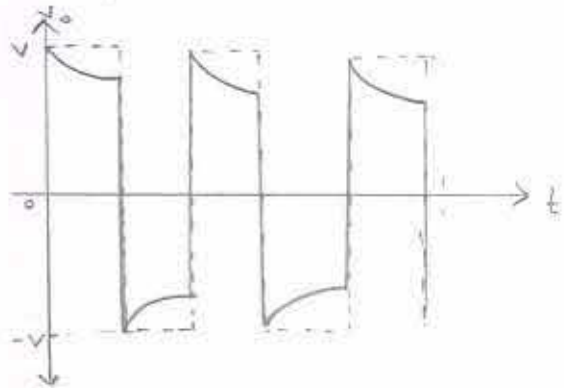
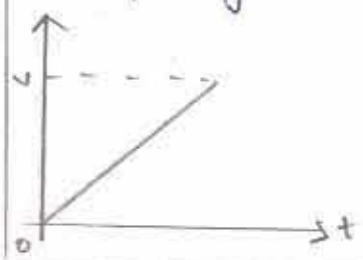
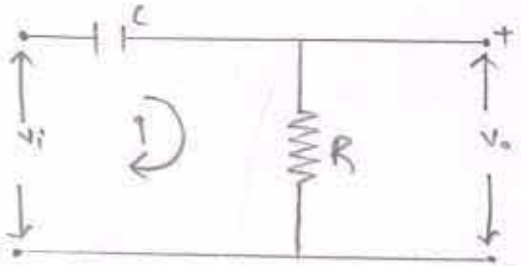
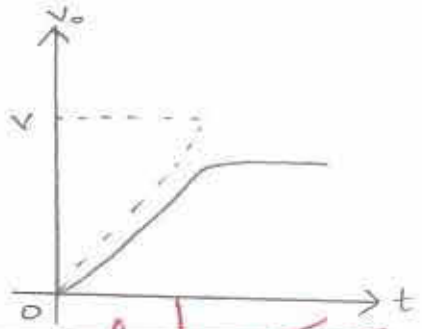
* Low Pass RC circuit

SL.No	Input Signal	circuit Diagram	Output waveform.
①	Step Signal 		
②	Pulse signal. 		
③	Square Signal 		

Sl No	Input Signal	circuit diagram	Output wave form
④	Ramp Signal 		RC >> T  RC <<< T 

* High Pass RC circuit *

①	Step Signal 		
②	Pulse Signal 		RC <<< T  RC >> T 

Sl.No	Input Signal	circuit Diagram	Output waveform.
③	Square Signal 		RC << T 
			RC >> T 
④	Ramp Signal. 		

G. Jayasree

17UR1D0404.

PDC - Assignment - 1

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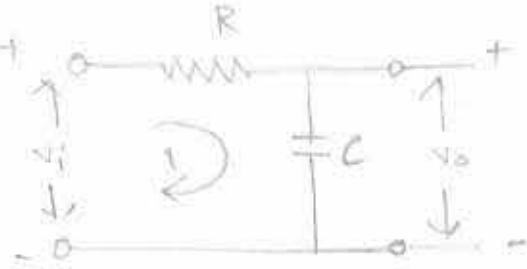
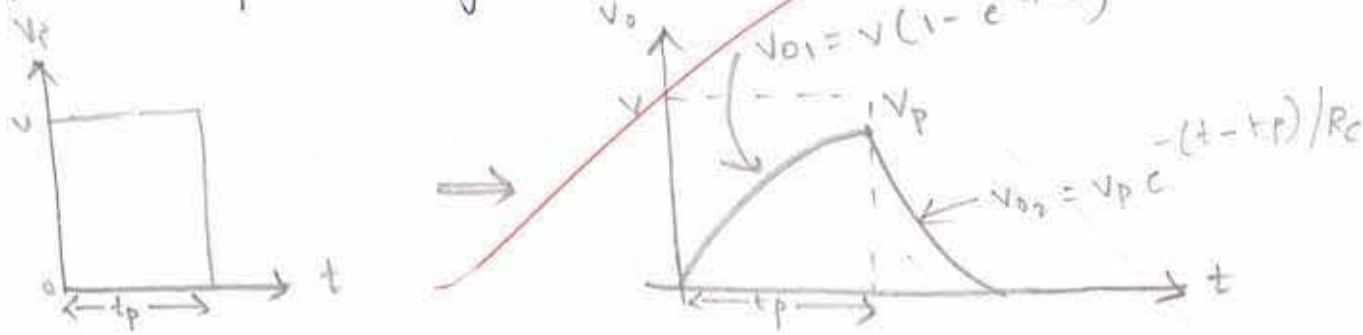
1) Draw the o/p of the low pass RC ckt for different time constant to pluse input & Square input Signal.



5 Marks
RC low pass CKt

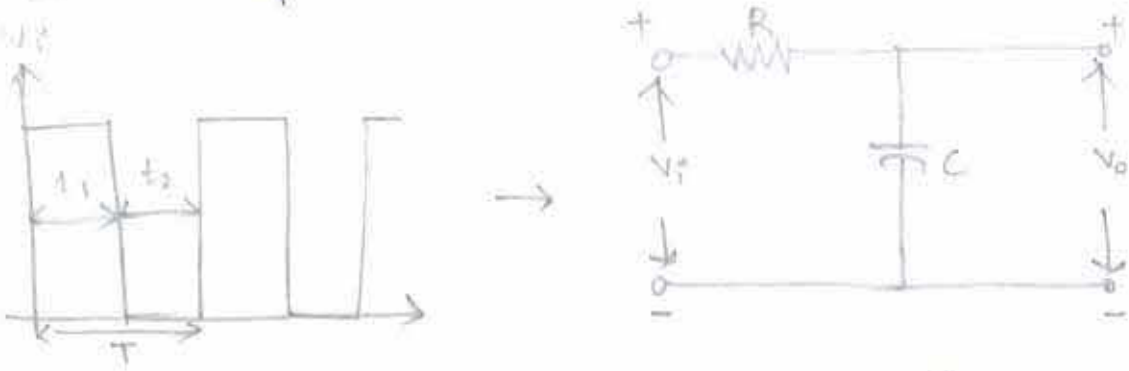
→ Since the reactance of a capacitor decreases with increase of freqeuncy & vice versa. It can seen that the capacitor offers much large impedance to low freqeuncy components pass out easily to o/p without any appreciable attenuation. Therefore the ckt is Low pass RC ckt.

→ Let pluse signal be applied to L.P.RC ckt.

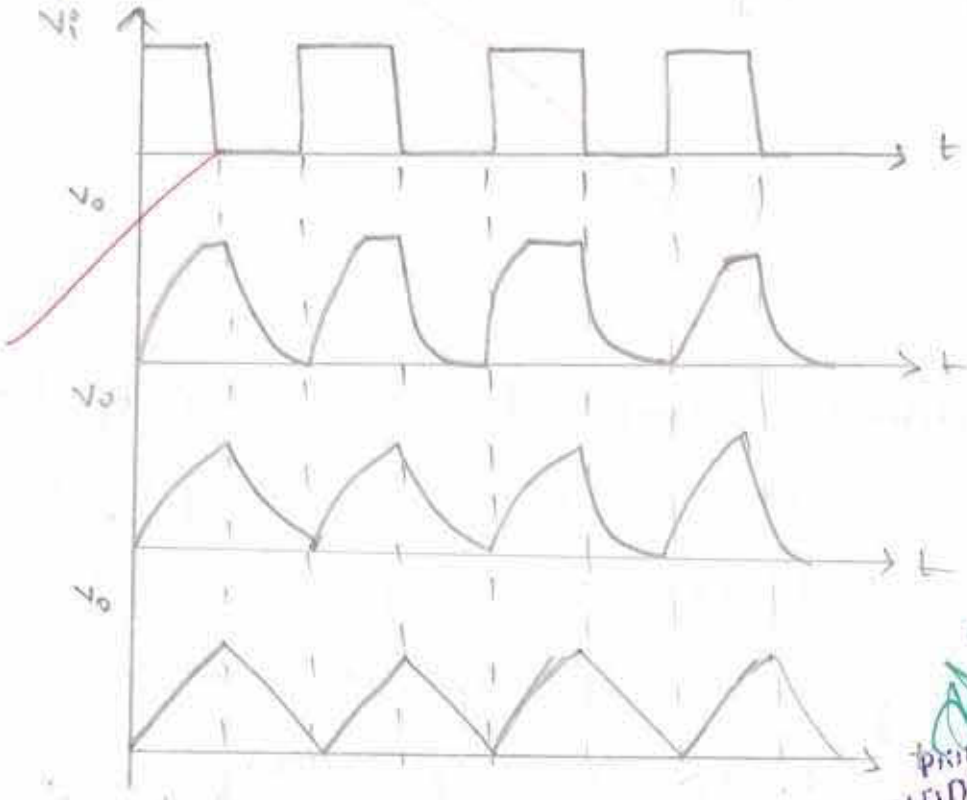


→ It is evident that for $t > 0$ but $< t_p$ the pluse width, the pulse voltage is exactly alike a step voltage and hence the o/p voltage increases exponentially from 0 to V_p at the end of the pulse. At $t = t_p$ the i/p voltage drops to zero & hence the o/p decreases exponentially and becomes zero at $t = \infty$ as shown in figure above.

→ Let the input signal be Square wave given to low pass RC ckt.



→ A Square wave is a periodic waveform which maintains itself at one constant level with respect to ground for time 't_1' & then changes abruptly to another level and remains constant ~~at~~ that level for time 't_2'. and repeats itself at regular interval of $T = t_1 + t_2$.



→ If the rise time tr is quite compared to T, there is no marked distortion of wave form the o/p wave form would be seen.

→ when the o/p voltage is exponentially increasing then, $V_{o_1} = V' + (V_1 - V')e^{-t/RC}$

→ when o/p voltage is exponentially decreasing then, $V_{o_2} = V'' + (V_2 - V'')e^{-(t-T_1)/RC}$.

→ when time constant is very large compared to periodic time. The exponentially curves beomes practically linear.

② Classify different types of clipper circuits and explain thier operation and also transfer characteristics.

→ They are different types of clipper circuits, mainly

① Diode clipper CKt

② Transistor clipper CKt.

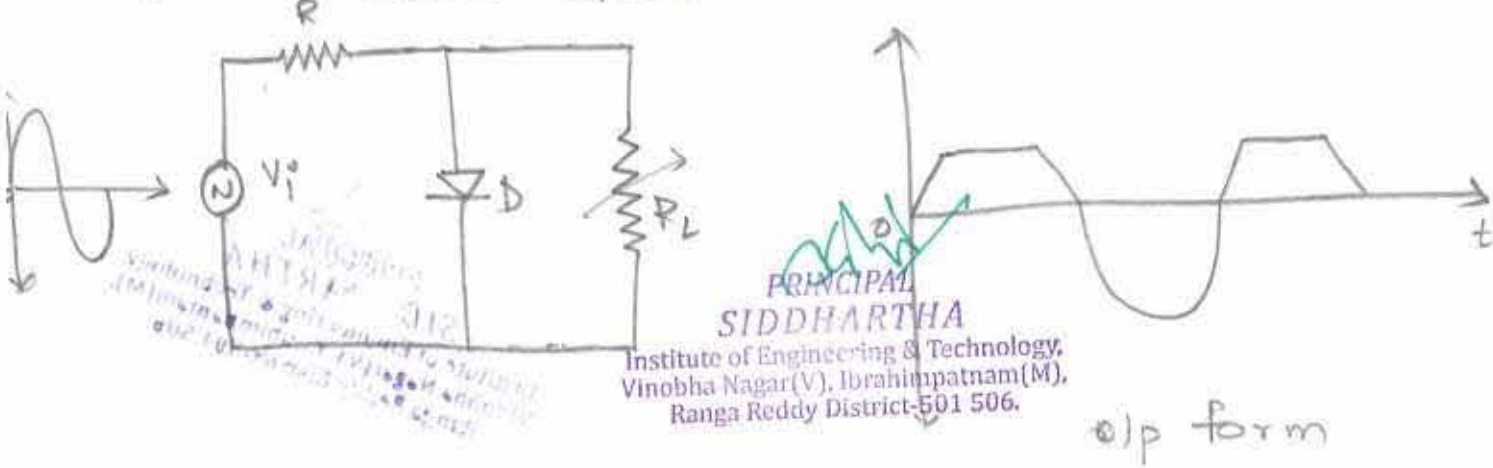
③ clipping at two Independent level CKts

① Diode clipper CKt :-

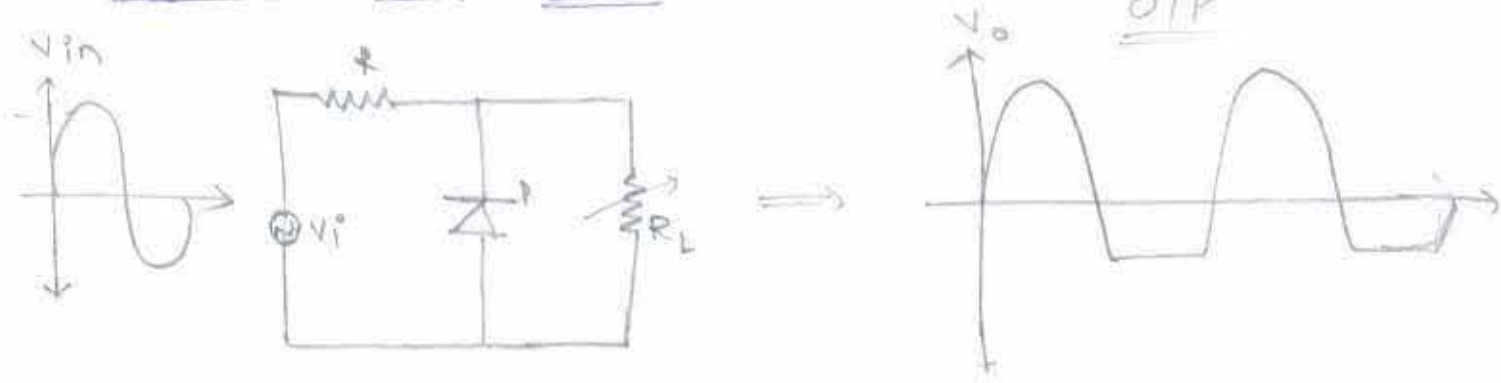
→ clipper is an electronic device which removes some portion of i/p signal. It is an voltage limitor.

→ Types of Diode clipper CKt

i) positive Diode clipper :-

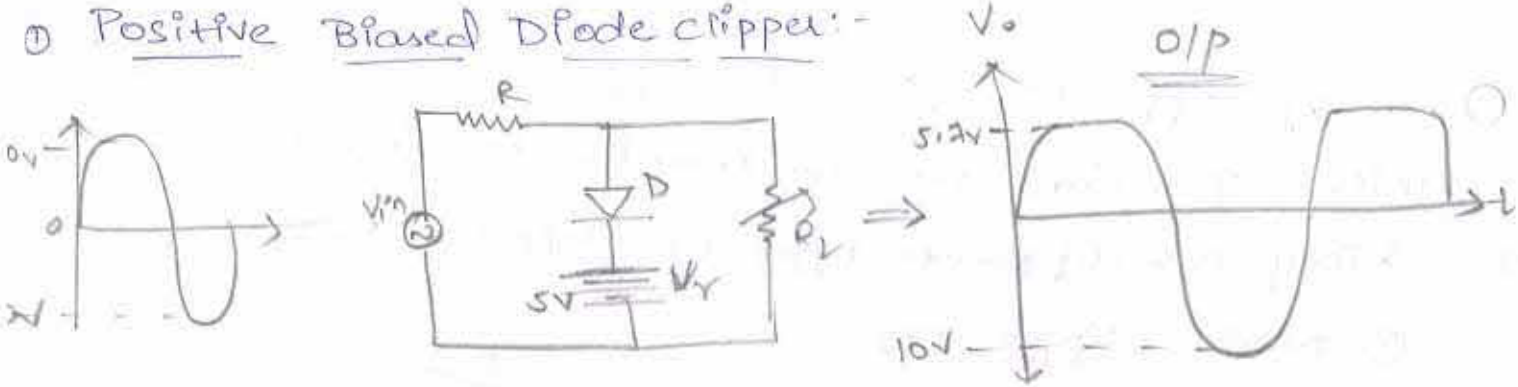


ii) Negative Diode clipper:-



iii) Biased Diode clippa:-

① Positive Biased Diode clippa:-

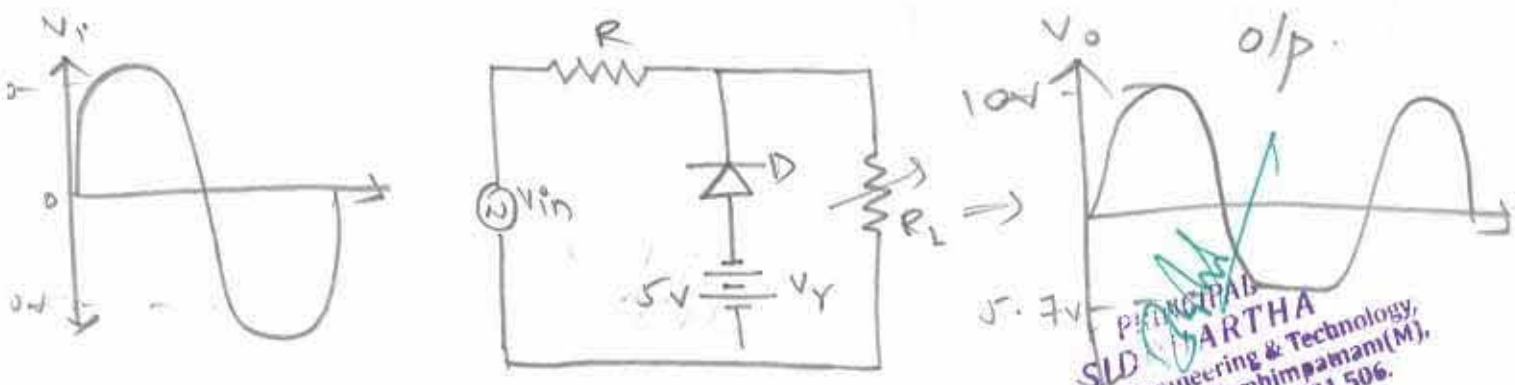


→ The i/p voltage is 10V and o/p voltage is 5V and Diode across D_1. The total amount of current pass through the load Resistance 'R_L'.

$\therefore V_o = 0.7V + 5V = 5.7V$

$\therefore V_o$ = Diode cut in Voltage + V_{Biase}

② Negative Biased Diode clipper:-

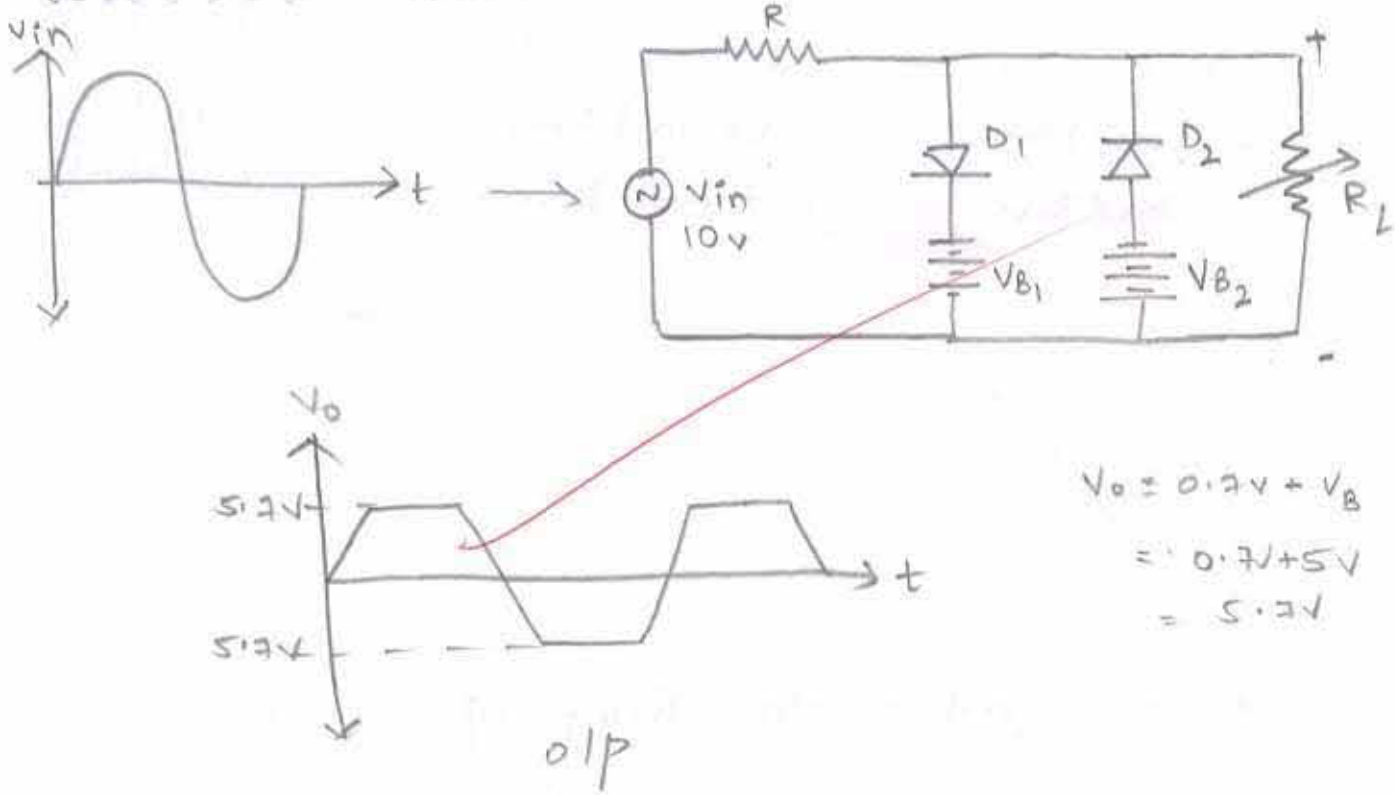


→ During +ve half cycle of AC Signal. The Diode D_1 is reverse Biase. The applied voltage is equal to the i/p voltage.

→ During -ve half cycle of AC signal. The Diode is forward Bias and it conducts. The voltage R_L is equal to Diode Resistance.

$$V_o = 0.7V + 5V = 5.7V$$

(iv) combination biased Diode clipper:-

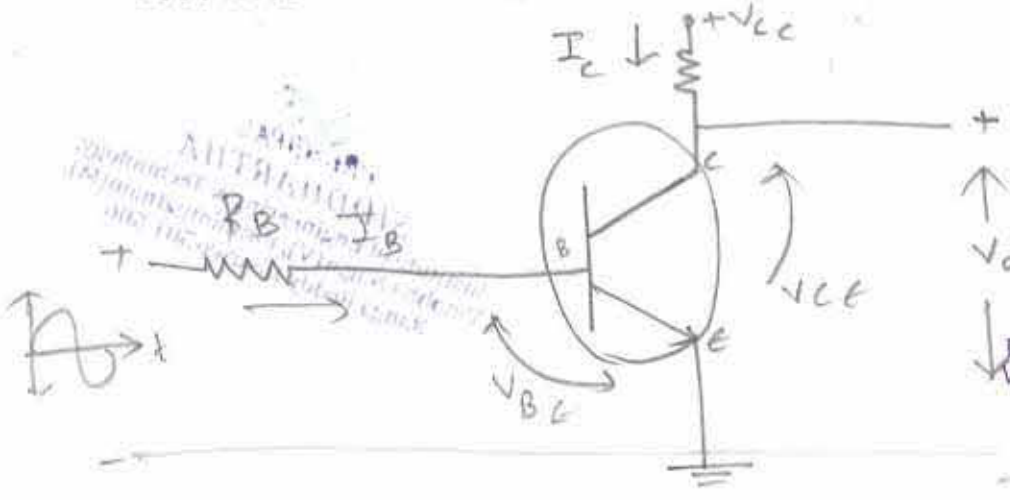


$V_o = 0.7V + V_B$

$= 0.7V + 5V$

$= 5.7V$

② Transistor clipper circuit:-



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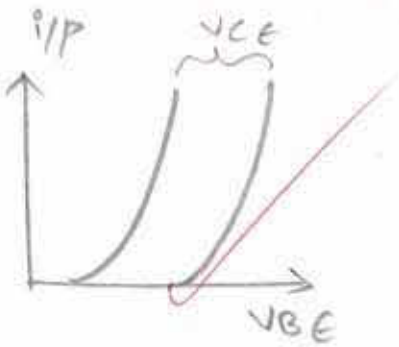
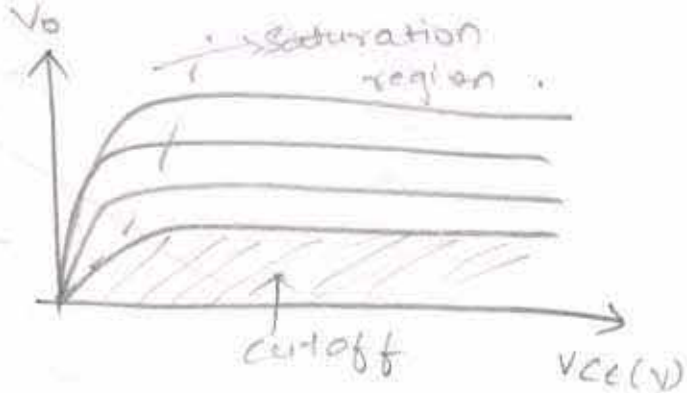
→ The transistor has two pronounced non-Linearities which may be used for clipping purpose. One across from cut-in into the active region, and second occurs when the transistor crosstram the active region to Saturation.

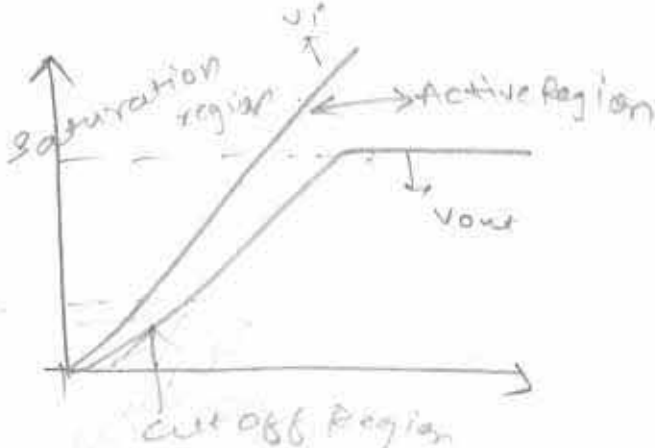
→ Transistor operating Regions:-

Transistor (emitter)	Transistor (collector)	operating Region
Forward Bias	Reverse Bias	Active Region
Reverse Bias	forward Bias	cutoff Region.
forward Bias	forward Bias	Saturation Region.





→ Input Signal is the Ramp i/p Signal:-



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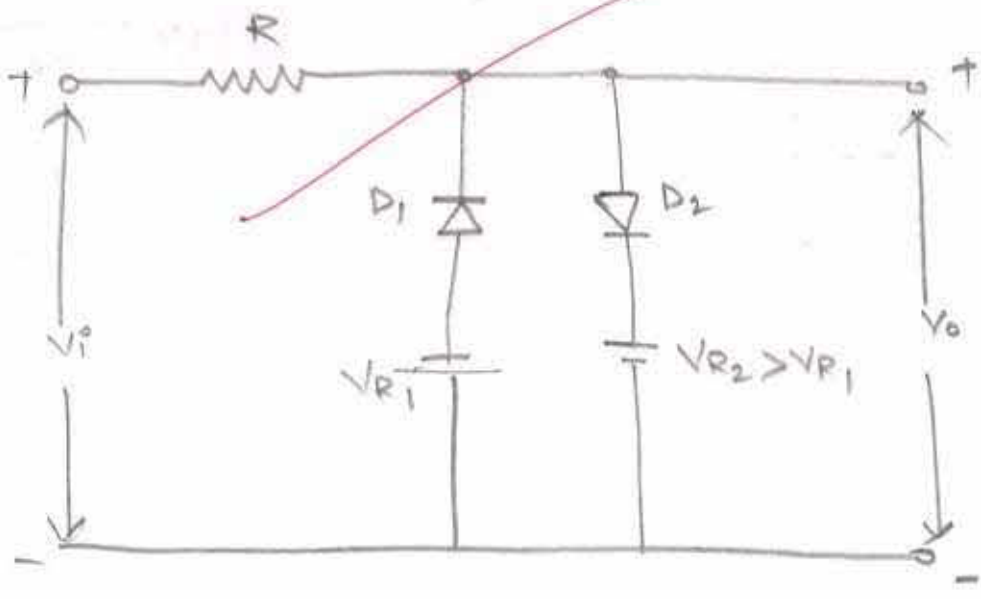
(3) Clipping at two Independent levels:-

→ The transfer curve has two breakpoints for double-ended limiting at independent levels.

→ $V_o(t) = V_i(t) = V_{R_1}$ and $V_o(t) = V_i(t) = V_{R_2}$.

Diode State during operating:-

i/p ($V_R(t)$)	o/p ($V_o(t)$)	Diode State
$V_i(t) \leq V_{R_1}$	$V_o(t) \leq V_{R_1}$	D_1 ON, D_2 OFF
$V_{R_1} < V_i(t) < V_{R_2}$	$V_o(t) = V_i(t)$	D_1 OFF, D_2 OFF
$V_i(t) \geq V_{R_2}$	$V_o(t) = V_{R_2}$	D_1 off, D_2 ON



→ if $V_i \leq V_{R_1}$

Diode D_1 is Reverse Bias

Diode D_2 is forward Bias

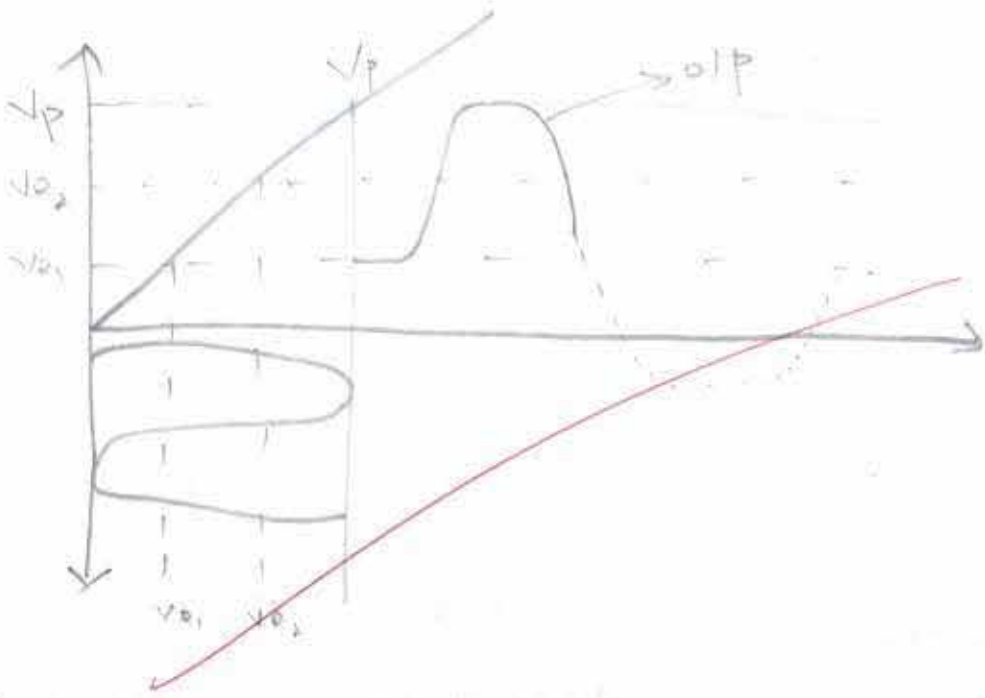
$V_o = V_{R_1}$

→ $V_i \geq R_2$

Diode D_1 is forward Bias

Diode D_2 is Reverse Bias

$V_o = V_{R_2}$



G. Jayasree

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PDC- Assignment-2

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Vinobha Nagar(V), Ibrahimpatnam(M),
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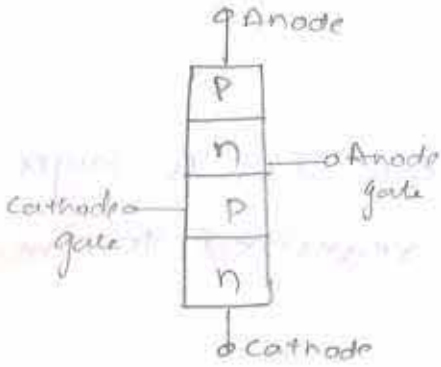
(5)

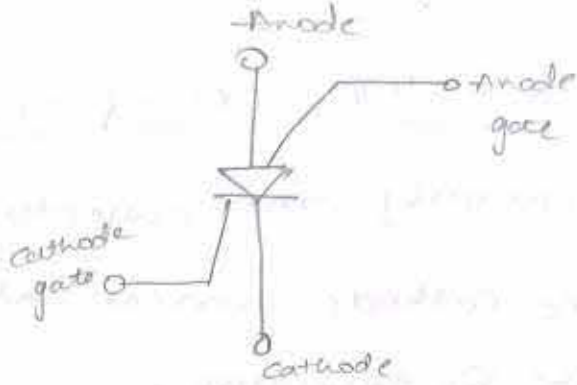
① Explain in detailed about Silicon Diode - controlled Switch circuits.

→ Silicon - controlled Switch circuits are the four - layer diodes, in which p and n-type layers are placed alternately as shown in fig (1a) Sequence can be either 'pnpn' or 'npnp'.

→ Here Anode current is used to turn-ON and turn-OFF the device.



Basic Construction



Graphic Symbol

→ from below circuit, if negative pulse is applied at the anode Gate, transistor 'Q_1' gets forward - biased and will turn - ON.

→ During ON - State transistor 'Q_1' gives large current I_{c_1} which turns - ON, the transistor 'Q_2' and this action repeats and in order to turn OFF the SCS, a positive pulse is applied at the anode Gate.

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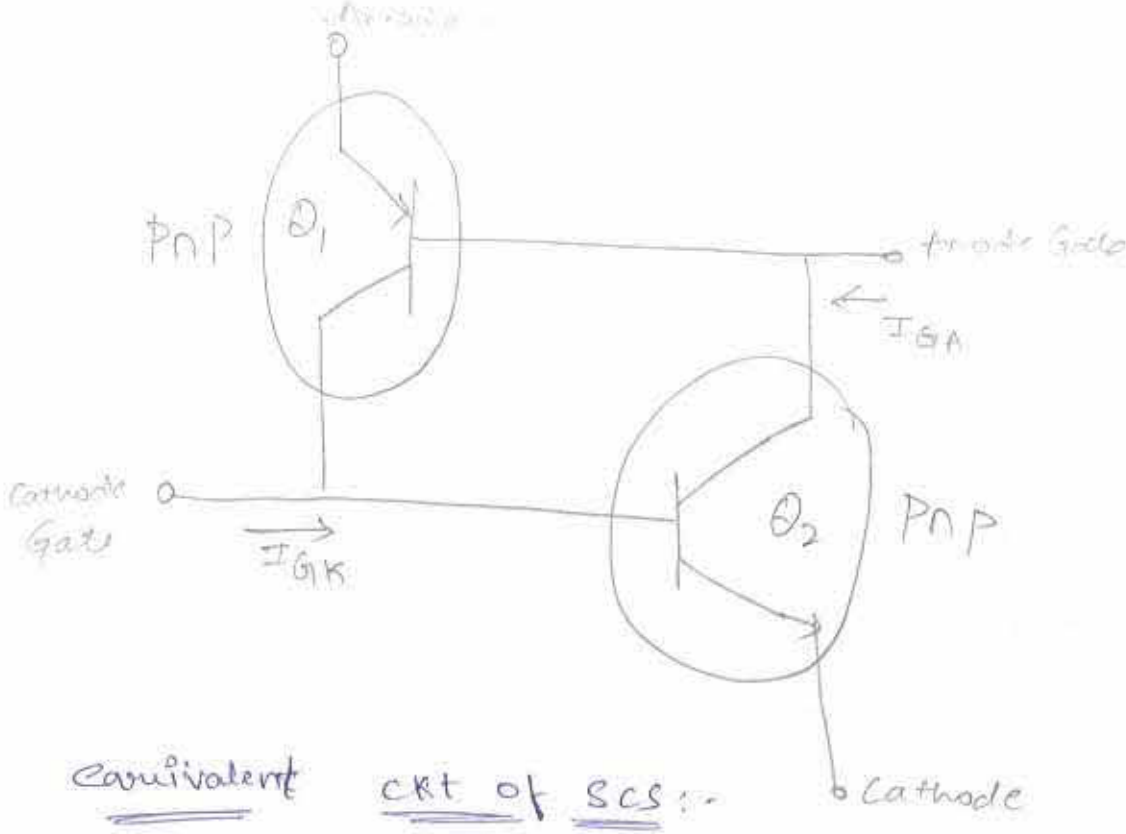
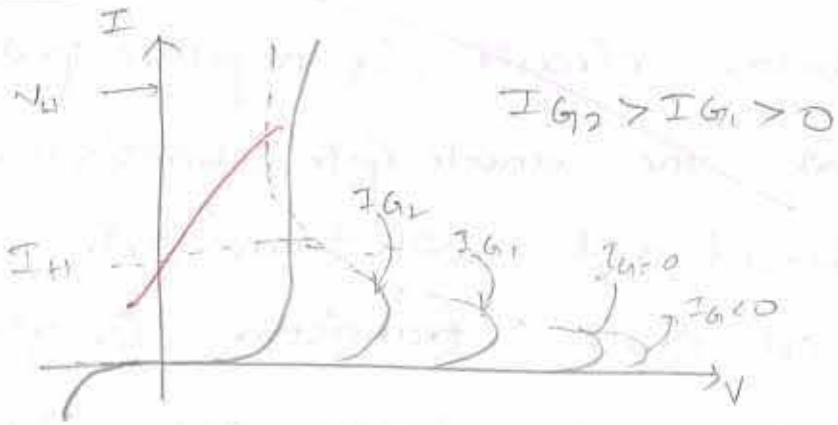


Equivalent ckt of SCS:-

→ Generally the collector current I_{C_1} is larger than the cathode current which is required to turn-ON the 'Q_2' transistor.

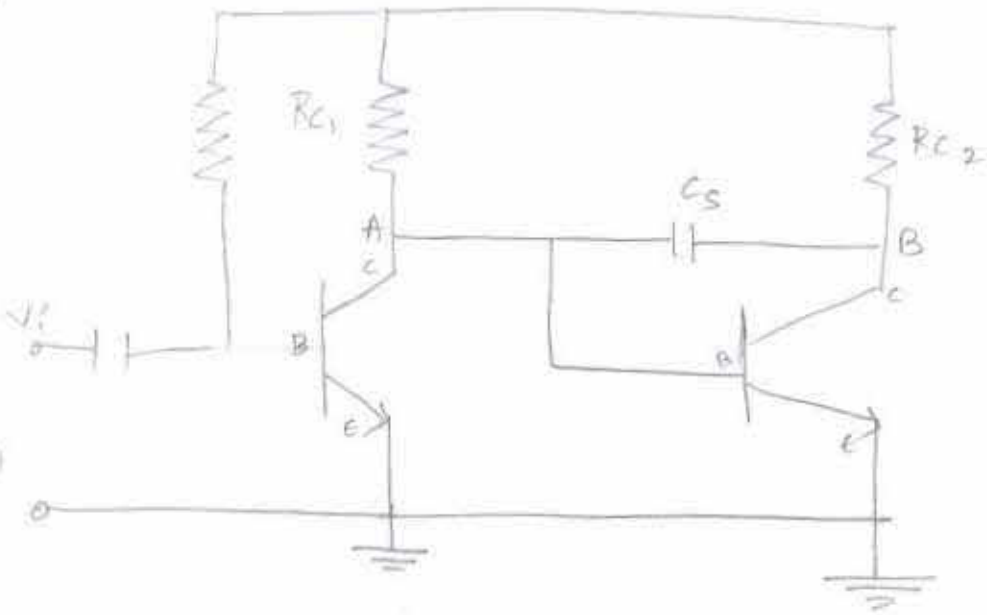
Characteristics of SCS:-



→ Volt-ampere characteristics of a three-terminal SCS illustrating that forward break-over voltage is a function of the cathode gate current.

2) Explain with neat Diagram for the time base Generator of Miller Sweep & Bootstrap ckt.

Any



→ Transistor Q_1 acts as ON-OFF switch, Q_2 is a high gain amplifier.

→ When the i/p 'V_i' is positive, Q_1 is ON in saturation. V_A becomes zero. $\boxed{V_A = 0}$

→ Transistor Q_2 remains OFF; $\boxed{C_S = V_{CC}}$

→ when i/p V_i is negative; Q_1 is OFF; 'A' tends to rise to V_{CC}.

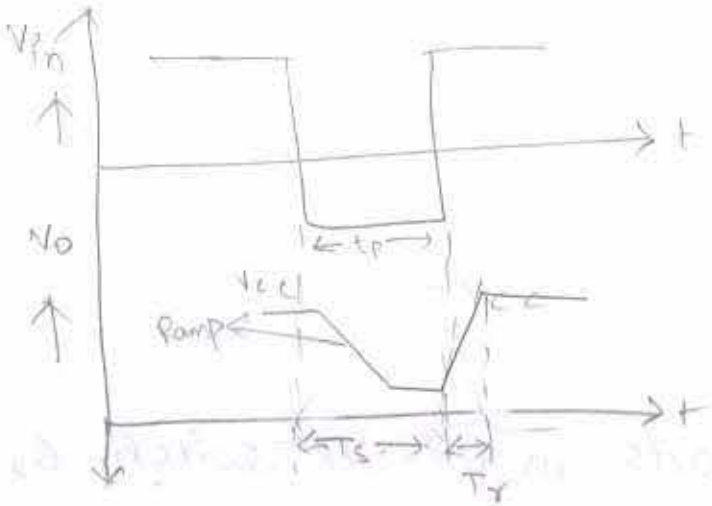
→ But due to 'C_S' present in the circuit, 'V_A' cannot rise to V_{CC} instantaneously.

→ With Q_1 OFF & A goes up, Q_2 becomes ON.

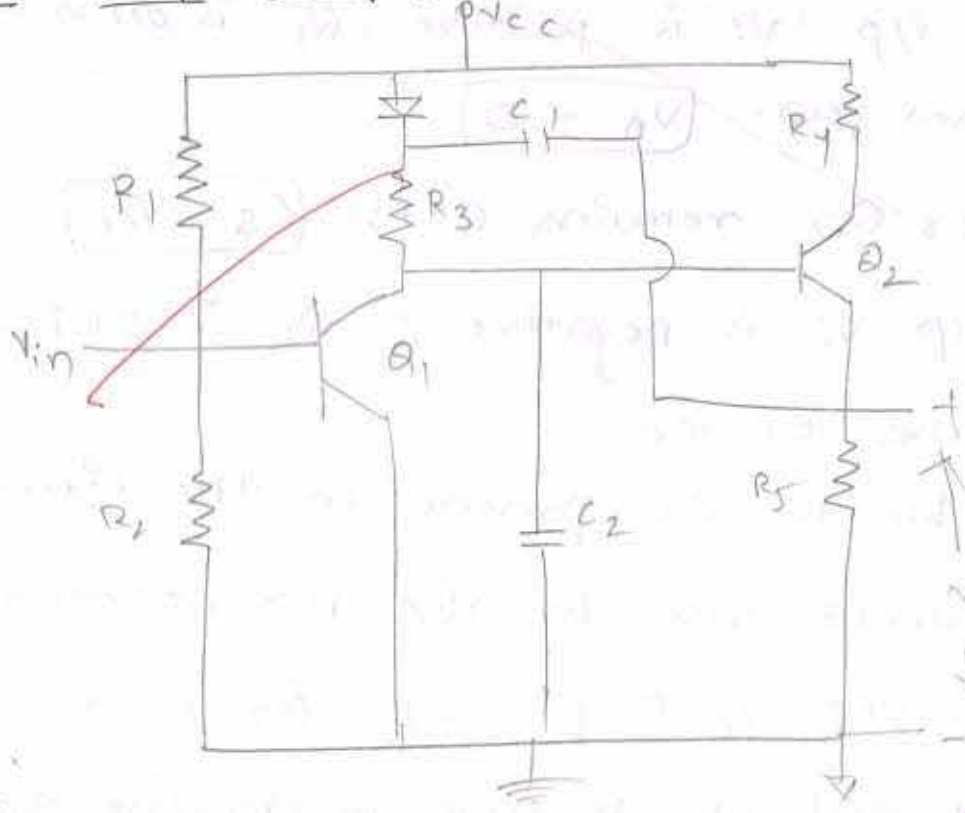
∴ Potential of B tends to decrease to zero, but due to C_S, V_B come down. Sosi Prasad

increases V_A and decreases V_B.

→ The voltage across the capacitor falls. The Result is that C_s discharges Linearly. Thus the voltage V_s across the capacitor C_s is a decreasing i.e, Negative going Ramp. (Negative feed back).



Boots Strap Sweep Time Base Generator:-



→ The transistor Q_1 acts as ON-OFF Switch and the transistor Q_2 is an emitter-follower.

→ The i/p 'Vi' is a pluse voltage or Rectangular wave

→ when 'Vi' is positive, transistor goes ON (i.e Q_1)

∴ $V_A = V_{CE(sat)}$

→ Q_2 is coupled to collector of Q_1. Hence point B becomes negative w.r.t V_{cc}, Diode D readily conducts $V_B \approx V_{cc}$

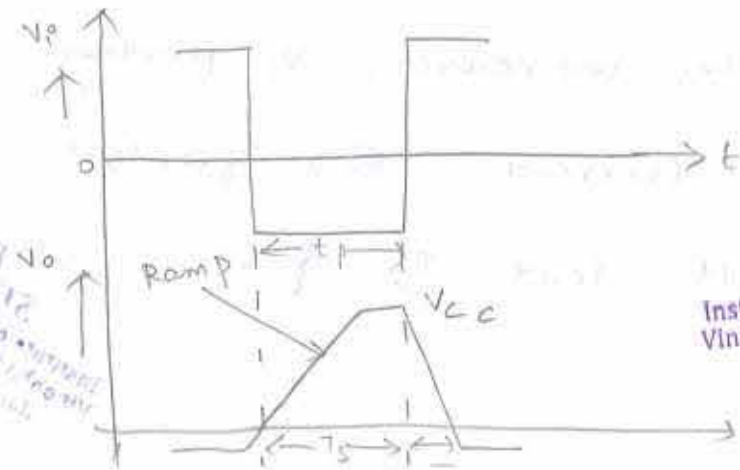
→ when V_i is negative, Q_1 is OFF. The 'A' Rises. This voltage increase at A is transmitted to B throgh Q_2 & Capacitor C_B. The result is potential of B also rises by same amount.

→ Since Both V_{cc} and R_{C_1} (i.e R_3) are fixed. So. $\frac{V_{cc}}{R_{C_1}}$ is constant. I is also constant

→ Since Q_1 is cut off collector current is zero, its impedance very high (Q_2)

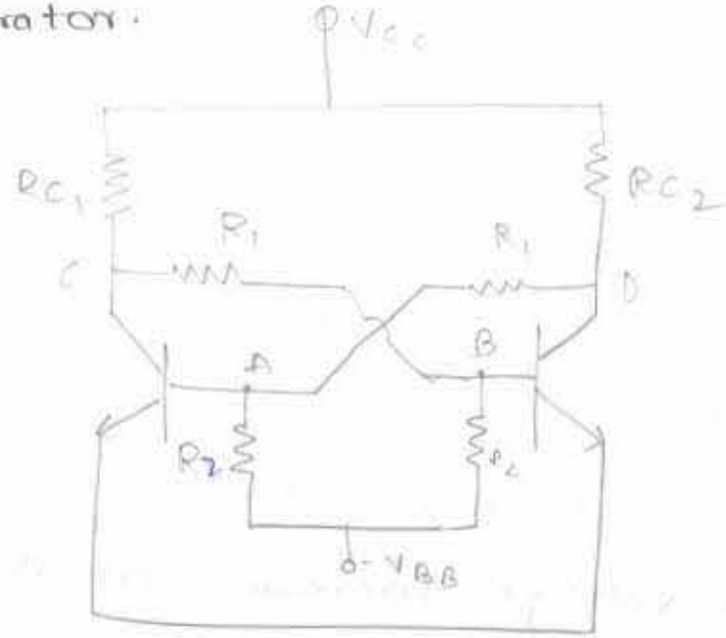
→ As this current flows through 'Cs' a ramp voltage is developed.

→ for emitter follower, voltage gain is unity. o/p is ramp.



5) Draw & Explain the working principle of bistable multivibrator.

Ans



→ When I_1 increases slightly, the voltage drop across the collector Resistance R_C, increases Since V_{cc} is fixed, at 'c' decreases, this has effect of decreasing the base current Q_2.

→ If I_2 decreases, the voltage drop $I_2 R_2$ decreases. Hence the voltage of 'D' point increases.

→ Due to V_D increase the base current Q_1 increases. This increases the collector current of Q_1 i.e I_1. I_1 further increases, $I_1 R_C$, drop further increases, V_c further decreases the base current Q_2 further decreases with result that I_2 further dc

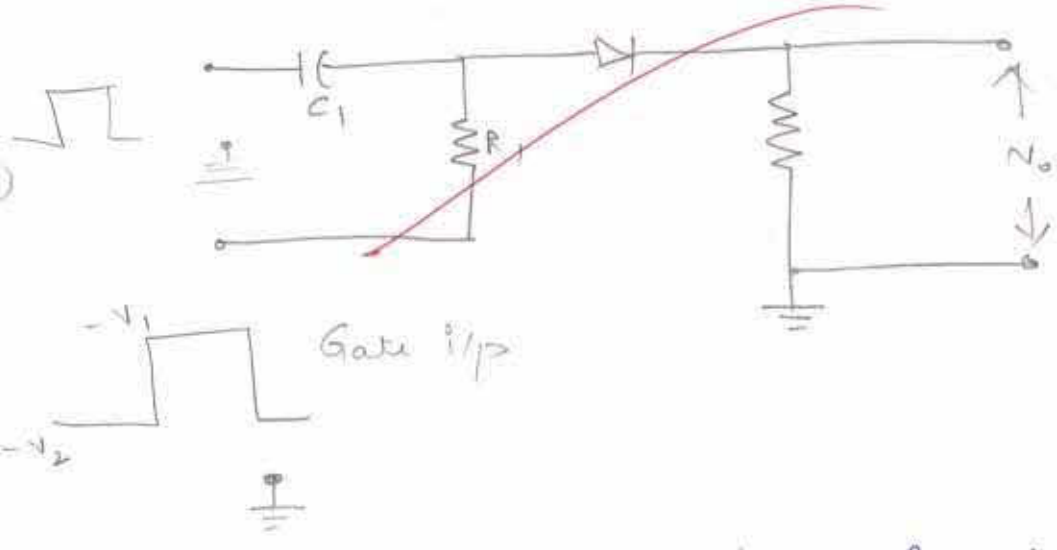
→ It can similarly be shown that I_2 increases even marginally similar sequence of operations would result and ultimately Q_2 would be ON, and Q_1 OFF.

→ Thus, when Q_1 is ON, Q_2 is OFF and when Q_1 is off, Q_2 is ON. It may be noted that both transistors are not ON or OFF simultaneously.

→ Thus, there are two stable states which remain indefinitely.

4) Explain the operation of unidirectional and bi-directional sampling gate

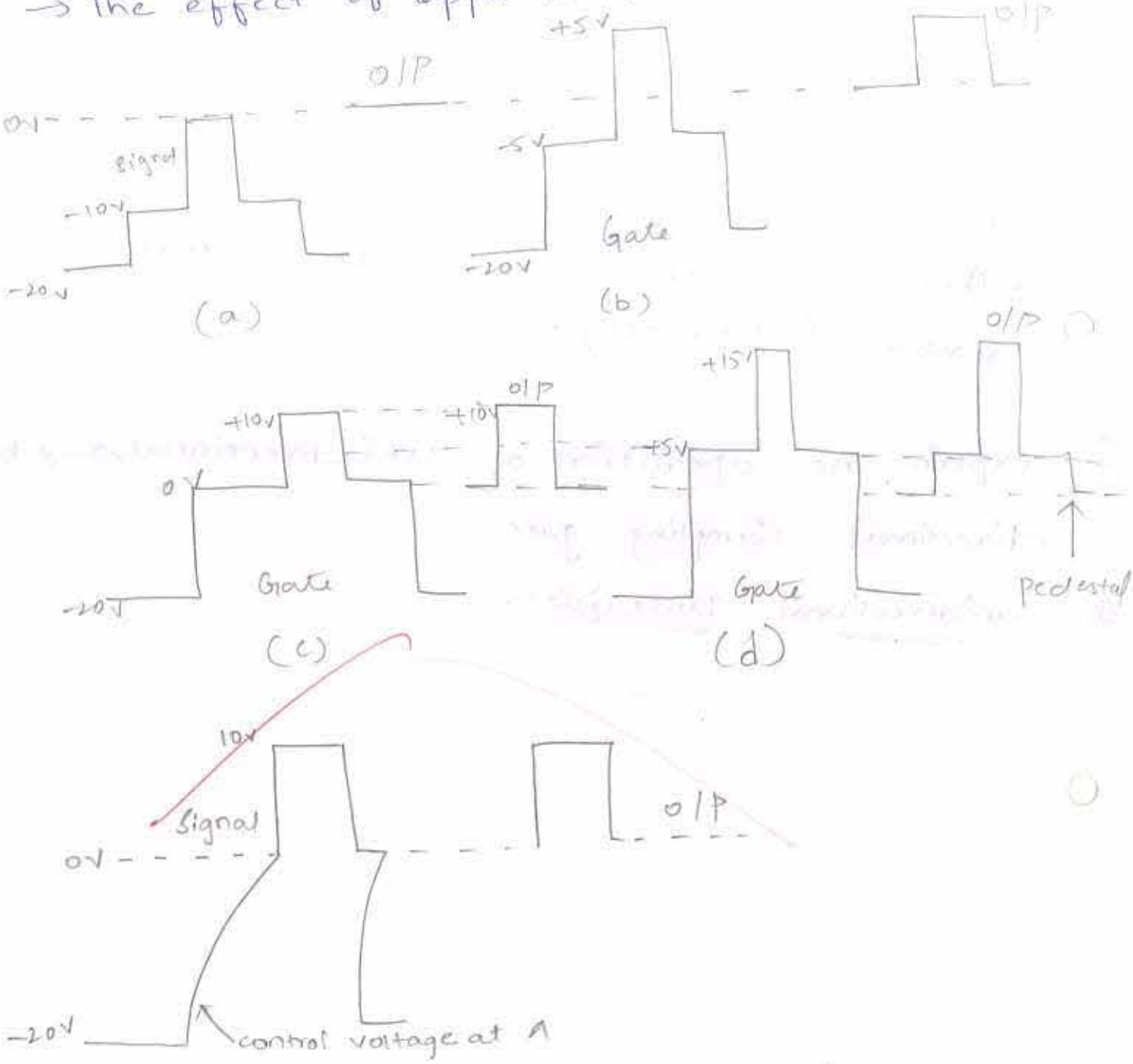
A) unidirectional Diode Gate:-



→ When the gating signal is at its lower level $-V_2$, the diode is heavily back biased and thus will be no o/p due to the i/p signal unless the peak amplitude of i/p signal is larger than the magnitude of this back-biasing voltage.

→ when gate signal is $-V_1$, a time-coincident signal i/p pulse may be transmitted to the o/p.

→ The effect of upper level is shown in fig below.



(e) Distortion of the control wave form.

→ fig(a); when gate pulse has $-V_2 = -20V$, $V_1 = -10V$. there is no o/p pulse at all.

→ fig(b); when $-V_2 = -20V$, $-V_1 = -5V$ ... o/p is +5V. pluse.

→ fig (c); when $-V_2 = -20V$, $-V_1 = 0V$, the o/p is +10V pulse

→ fig (d); when $-V_2 = -20V$, $-V_1 = 5V$, the o/p is 10V pulse is superimposed on a pedestal of +5V.

→ Since unrealistic of fig, because of R_1C_1 network constitutes an integrating network for the gate waveform; therefore gating signal will have exponentially rising & falling edges as in fig (c).

Bi-directional Sampling Gate:-

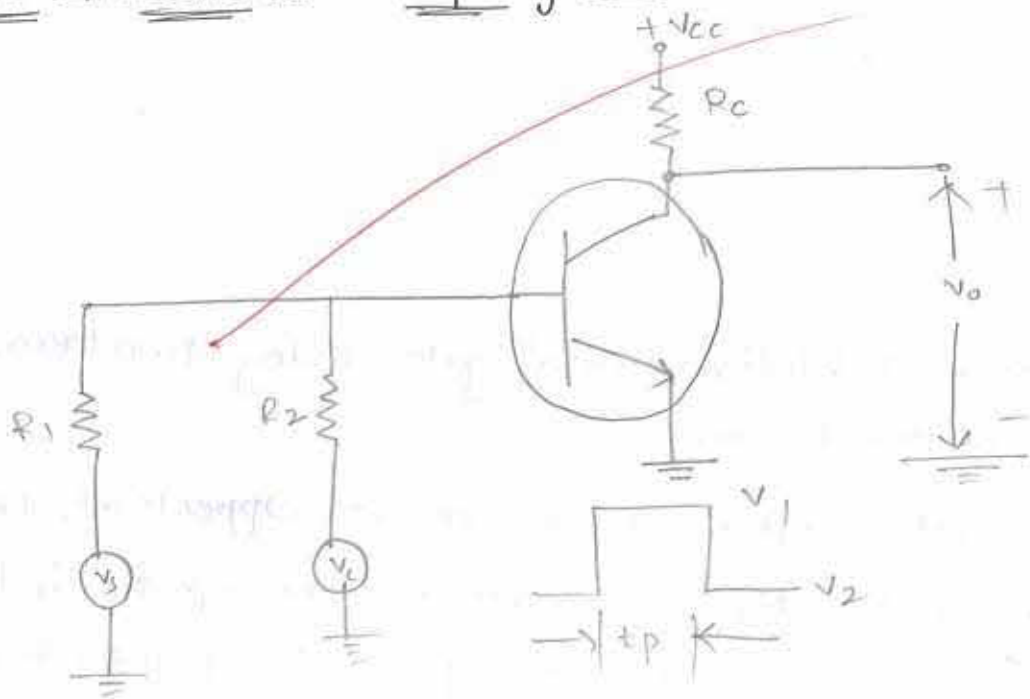


fig. (a)

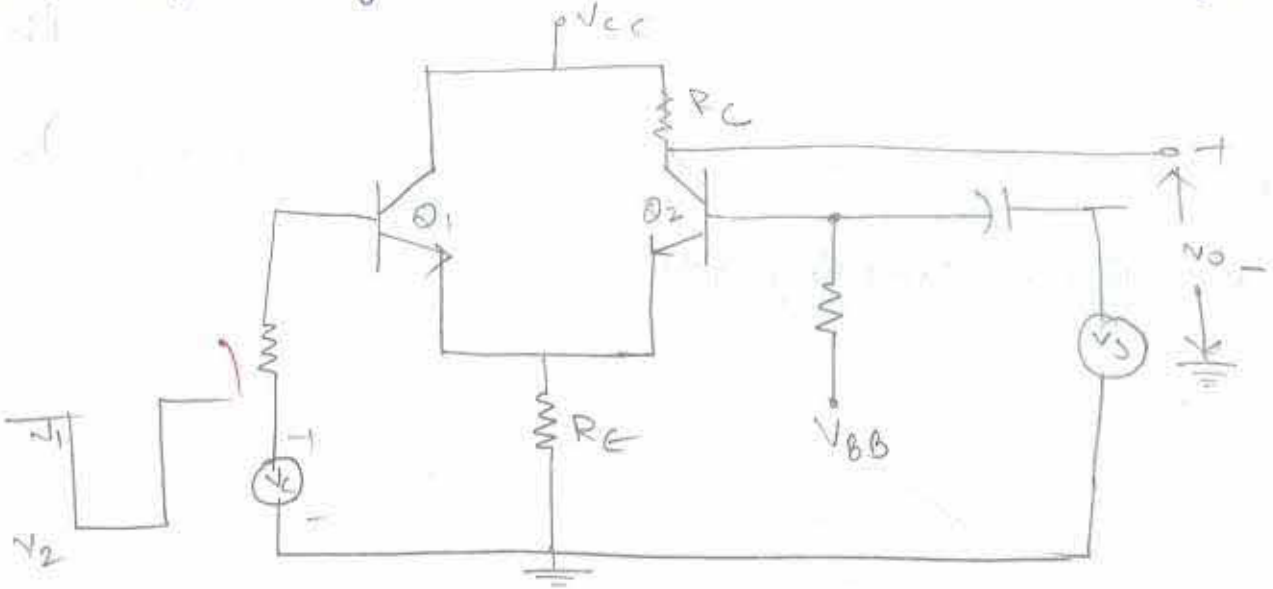
→ In fig (a); the signal voltage V_s and the control voltage V_c are applied through the summing resistors R_1 and R_2 to the base of a transistor.

→ when gating is at its lower level V_2, the transistor is well below cut-off.

→ when the gating signal is at the upper level V_1, the bias brings the transistor into the active region

→ so, as long as the gating signal is at its upper level, signals of either polarity appearing at the base will be sampled and will appear amplified at o/p.

→ Hence fig (a) acts as a bidirectional gate.



→ Fig (b) shows a bidirectional gate using two transistors which are emitter coupled.

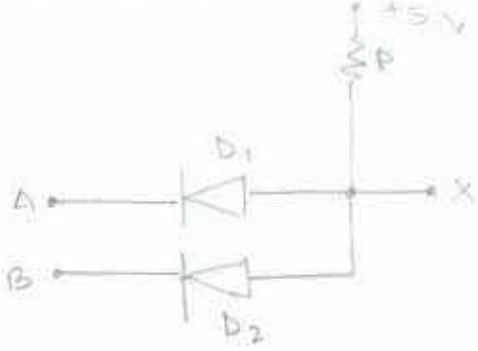
→ when the Gate signal V_c is at its upper level, the transistor Q_1 is ON, the current through R_E is large enough to raise the emitter voltage to the point where Q_2 is cut-off.

→ when the control signal V_c is at its lower level Q_1 is cut off & Q_2 is free to operate as an amplifier stage.

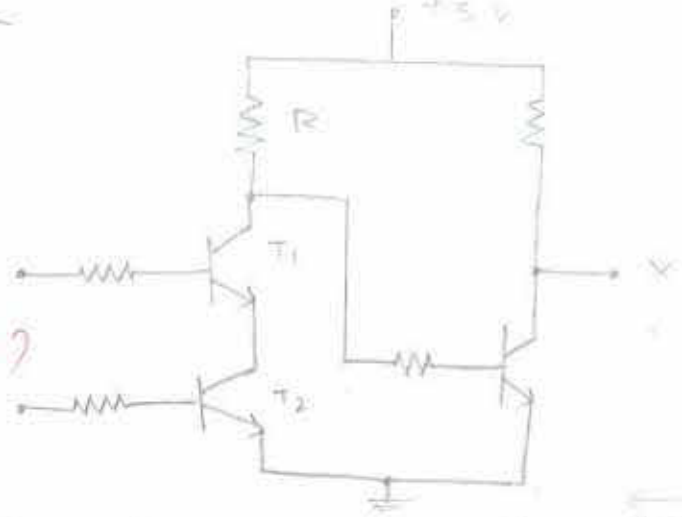
→ The signal V_S appears at the output amplified.

5) Realize AND Gate and OR gate using Diode & transistor.

Ans (i) AND Gate Realization:-



(a) two i/p diode AND Gate (DL)



(b) Two i/p transistor AND Gate (RTL)

→ When both A & B are low; i.e; A=0V & B=0V, both the diodes D_1 & D_2 are ON. current flows through R, D_1 & D_2

→ Almost all the supply voltage drops across R. Hence, the o/p voltage is X=0V (logic 0)

→ when, A=0V, B=5V; D_1 is ON, D_2 is off. current flows through R and D_1 and same happens i.e, X=0V

→ when; A=5V & B=0V, D_1 is off, D_2 is ON. Again Supply voltage drops across R. o/p voltage X=0V.

→ when A=5V & B=5V, Both D_1 & D_2 off. No current flows through R. Hence o/p voltage X=5V (logic 1)

i/p A	i/p B	o/p X
0	0	0
0	1	0
1	0	0
1	1	1

Truth Table:-

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Principal

→ when A = +5V & B = 0V, Here D_1 is F.B & D_2 is R.B. current flows through D_1 & R i.e $\boxed{X = 5V}$

→ When A = 0V & B = +5V, D_1 is OFF and D_2 is ON. current flows through D_2 and R and the o/p voltage $\boxed{X = 5V}$ (logic 1).

→ when A = +5 & B = +5V, Both D_1 & D_2 are ON, current flows through D_1 & D_2 and R and o/p is $\boxed{X = +5V}$.

Truth Table:-

Inputs		O/P
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

→ In transistor OR Gate (RTL OR gate), when A = 0V and B = 0V, Both T_1 & T_2 are OFF. T_3 gets enough base drive ; $\boxed{X = 0.3V} \simeq 0V$ (logic 0).

→ when A = 0V and B = 5V, T_1 is OFF & T_2 is ON current flows through T_2 and T_3 is OFF. $\boxed{X = +5V}$ (∵ no voltage drop across it).

→ when A = 5V & B = 0V, T_1 is ON & T_2 is OFF and T_3 is OFF. so no voltage drop across it

$\boxed{X = +5V}$

→ when A = 5 V and B = 5 V, Both T_1 & T_2 are ON. current flows through T_1 and T_2 and T_3 is OFF, since T_3 does not get enough base drive. no current flows through its collector resistance Rc. so no voltage drop across it. Hence

$X = +5V$.

PRINCIPAL
SIDDHARTHA
Institute of Engineering & Technology,
Vinobha Nagar(V), Ibrahimpatnam(M),
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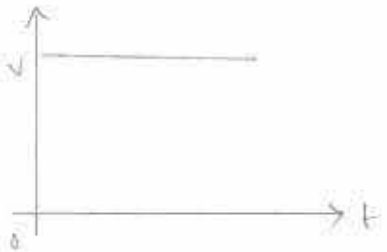
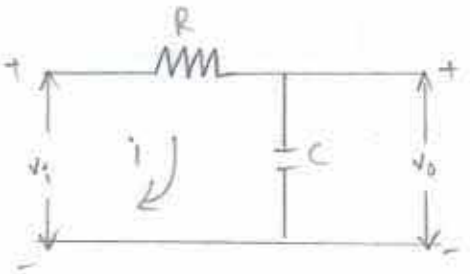
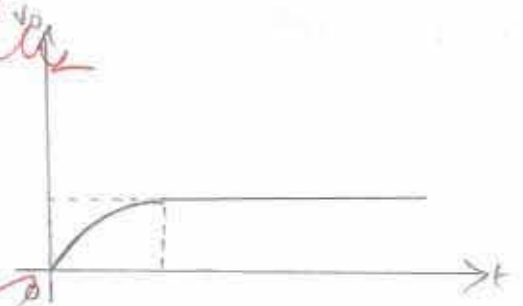
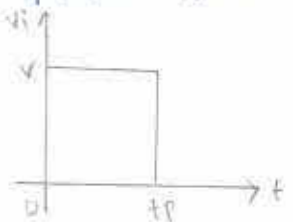
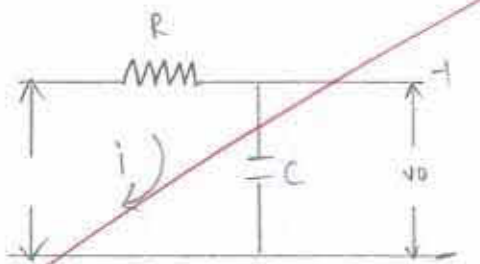
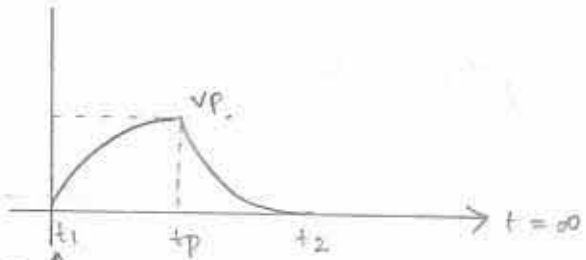
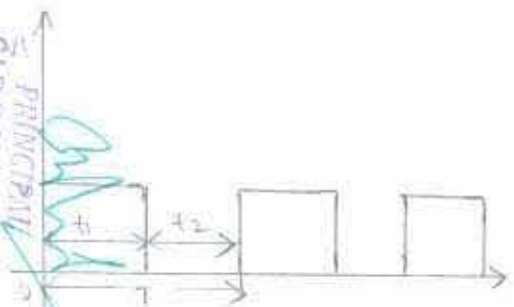
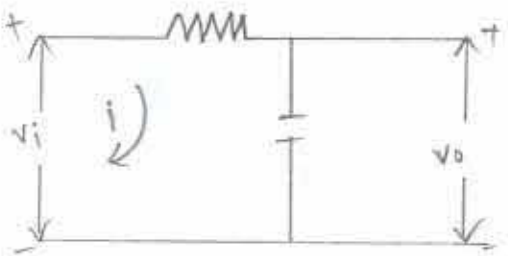
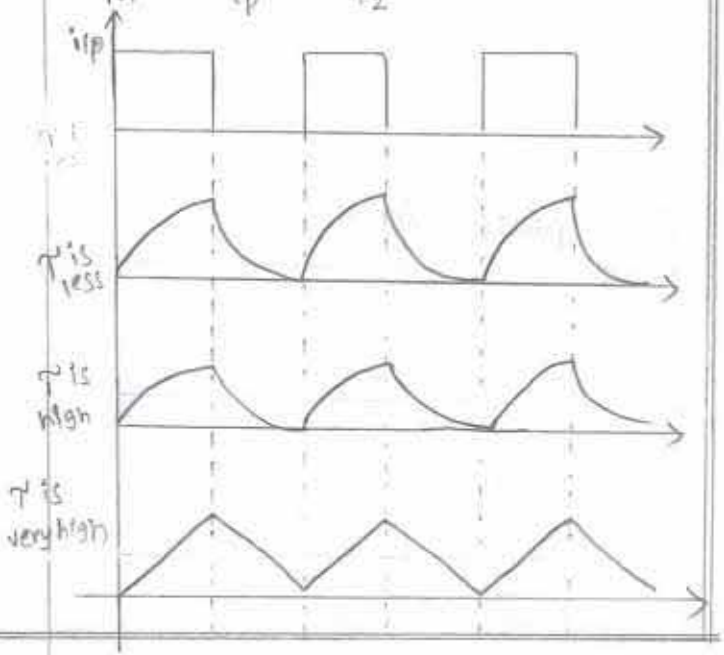
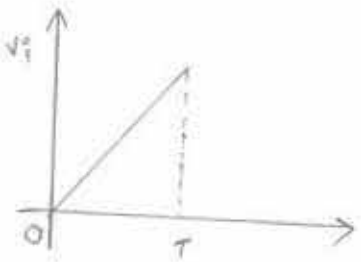
Assignment-1 PDC

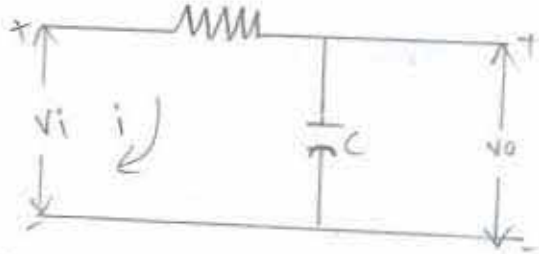
P. Ramya
17TP1A0465

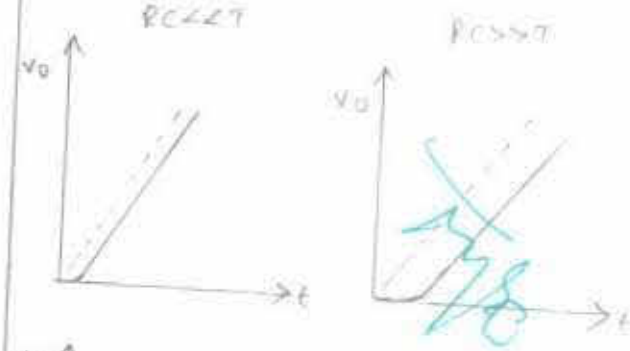
5/5

S.No	Input Signal	Circuit	Output Signal
1.	Step Signal. 		
2.	pulse Signal 		
	Sawtooth Signal. 		

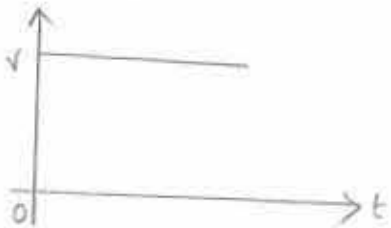
4. Ramp Signal

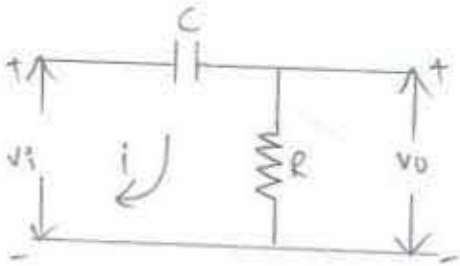


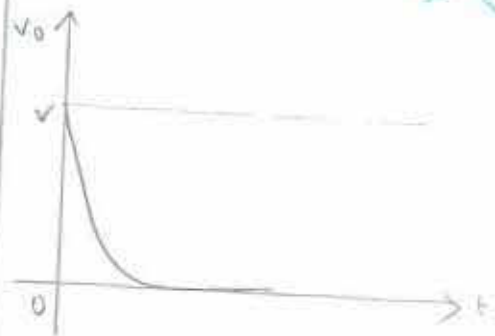




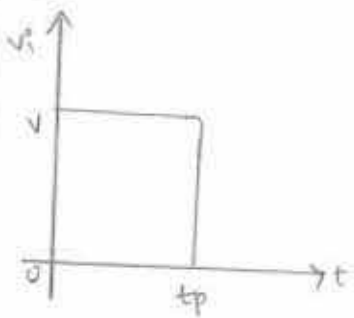
5. Step Signal.

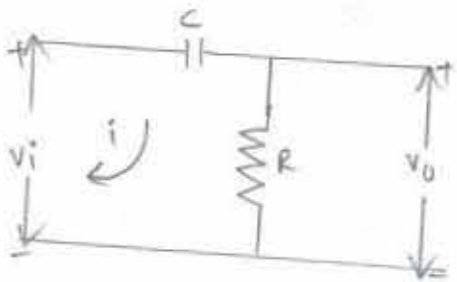


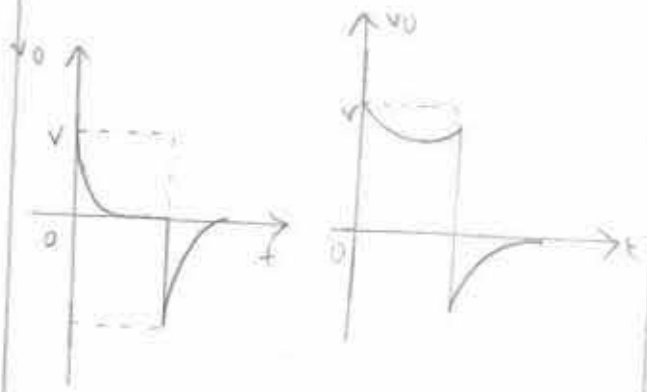


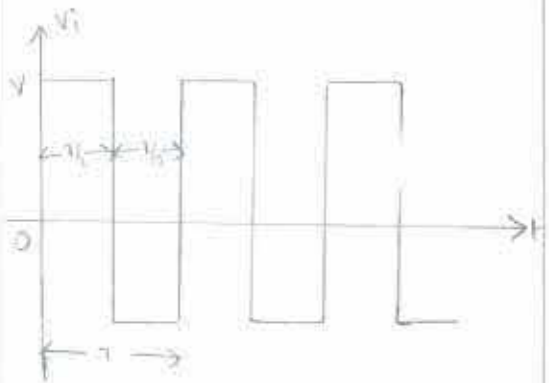
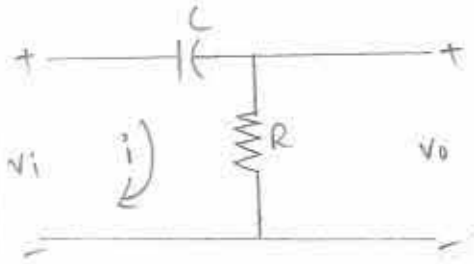
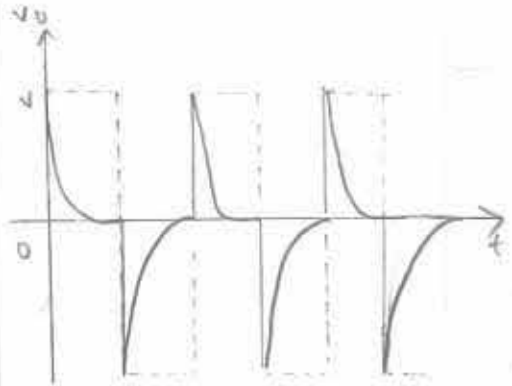
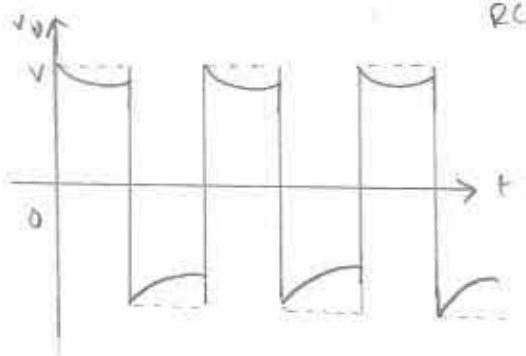
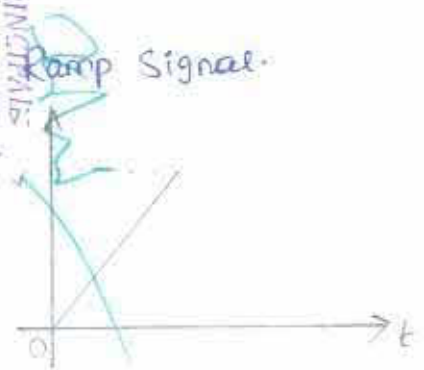
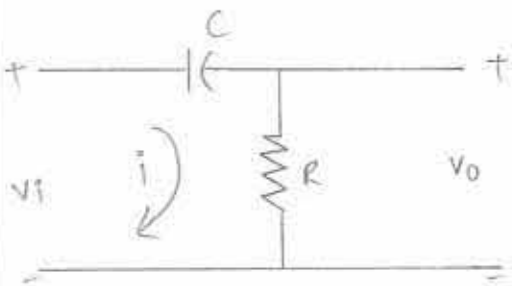
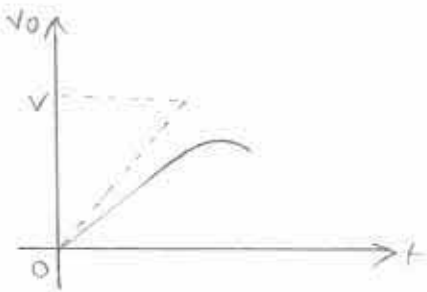


6. pluse Signal.





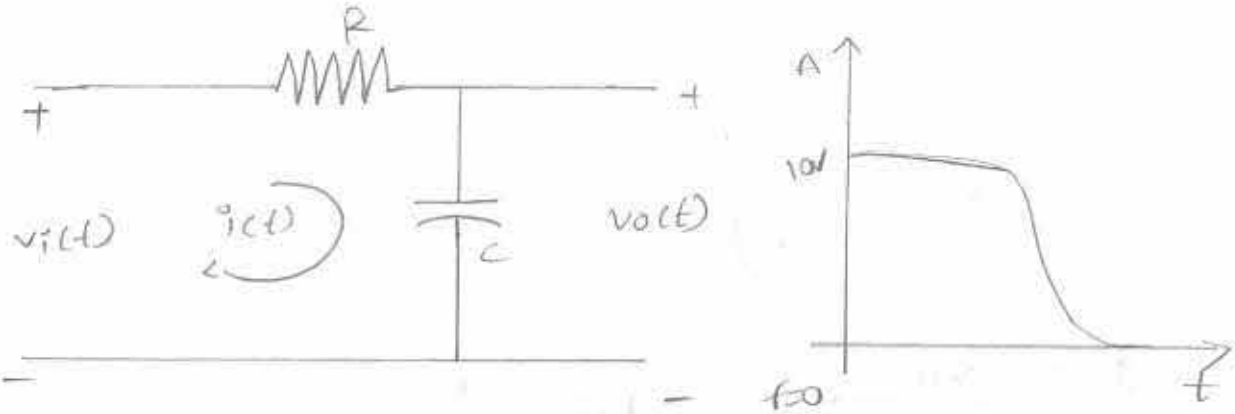


S.NO	Input	Circuit	Output Signal
7.	Sawtooth Signal 		RC<<T  RC>>T 
	Ramp Signal. 		

P Kamya
17TP1A0465

① Draw the o/p of the low pass RC circuit for different time constant to pulse i/p, square i/p.

* low pass RC circuit:-



→ As above the circuit is lowpass ckt is only allows the low frequency signal and attenuation high frequency signal for low frequency signal.

$f=0 \quad X_C = \text{high}(\infty) \uparrow \; ; \; X_C = \frac{1}{2\pi fc}$

→ for high frequency signal.

$f = \text{high}, \; X_C = \text{low}(0) \downarrow$

→ for low frequency signal capacitor acts as open circuit so we can measure the voltage across the capacitor.

→ as frequency is very low '0' we get max. voltage and frequency increases voltage decreases linearly.

$V_O = IR \quad — (1)$

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Ranga Reddy District-501 506.

$$I = \frac{V_{in}}{R_T} = \frac{V_{in}}{R - XC}$$

$$I = \frac{V_{in}}{R - \frac{J}{2\pi fC}}$$

$$I = \frac{V_{in}}{R\left[1 - \frac{J}{2\pi RfC}\right]}$$

$$I = \frac{V_{in}}{R\left[1 - \frac{Jf_1}{f}\right]} \qquad f_1 = \frac{1}{2\pi RC}.$$

$$V_0 = \frac{V_{in}}{R\left[1 - J\left(\frac{f_1}{f}\right)\right]} \times R$$

$$V_0 = \frac{V_{in}}{\left[1 - J\left(\frac{f_1}{f}\right)\right]}$$

$$\frac{V_0}{V_{in}} = \frac{1}{\left[1 - J\left(\frac{f_1}{f}\right)\right]}$$

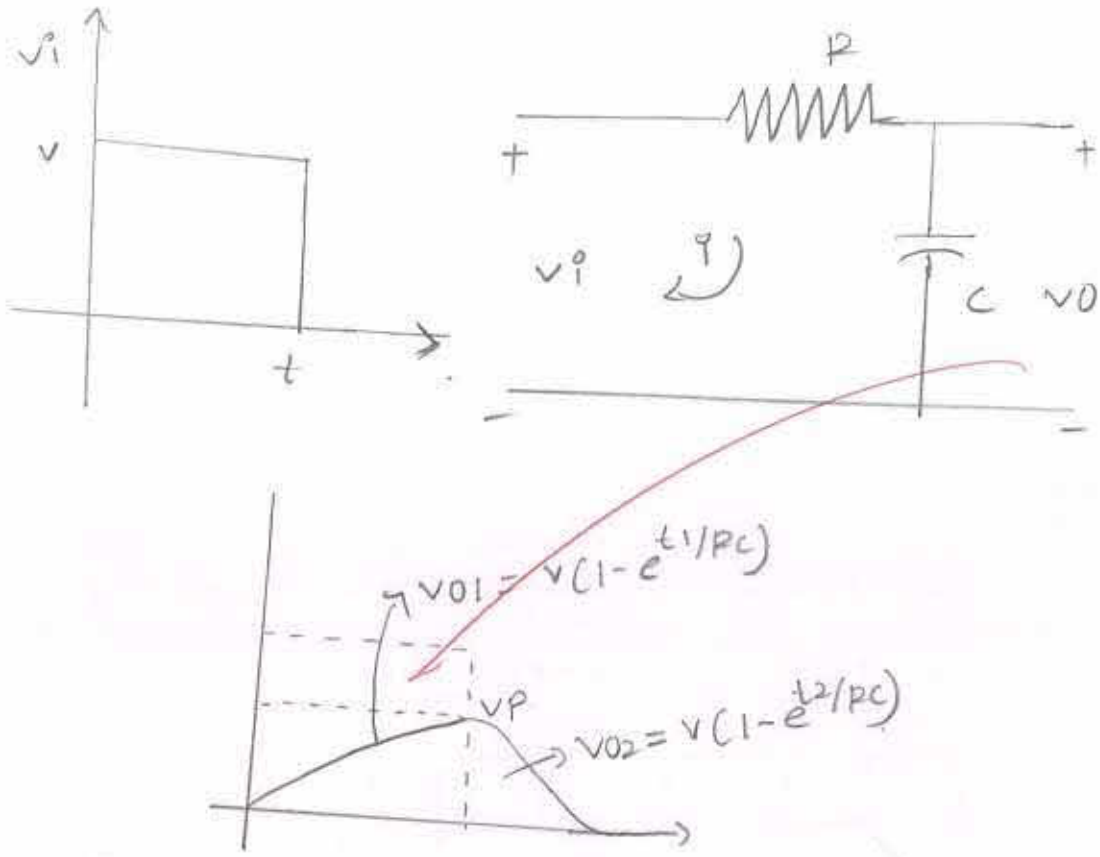
$$\text{Gain}(A) = \frac{V_0}{V_{in}} = \frac{1}{\left[1 - J\left(\frac{f_1}{f}\right)\right]}.$$

$$\left|\frac{V_0}{V_{in}}\right| = \frac{1}{\sqrt{1 + \left(\frac{f_1}{f_2}\right)^2}}.$$

at $f_L = f$.

$$\left|\frac{V_0}{V_{in}}\right| = \frac{1}{\sqrt{1+1}} = \frac{1}{\sqrt{2}} = 0.707.$$

* Response of low RC circuit for pulse input:-



$\tau = RC$ V = Amplitude of I/P signal.

→ If the constant RC of ckt is very large at end of pulse v_0 is $V(1-e^{-t/RC})$ and O/P will decrease to zero from this $\tau = RC$

it takes less time to charge - is "$V_p < V$"

τ = 20ms capacitor slowly charing.

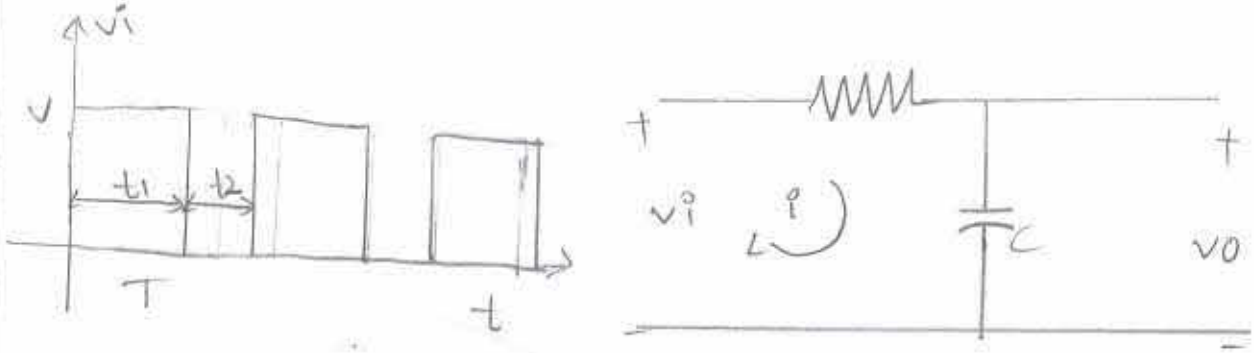
$$V_{O1} = V(1-e^{-t_1/RC})$$

$$V_{O2} = V(1-e^{-t_2/RC}) .$$

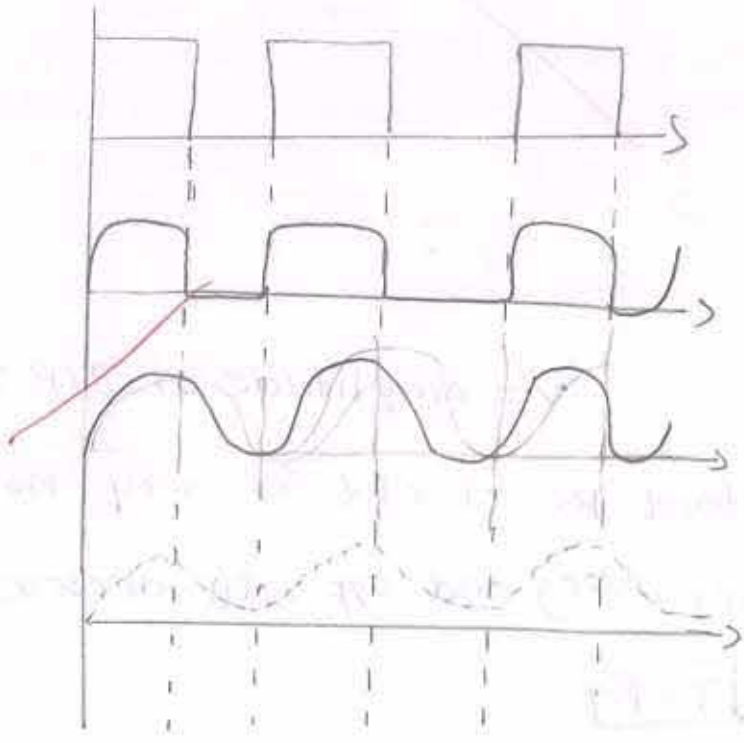
$$t_2 = t - t_p$$

$$v_{o_2} = V\left[1 - e^{-(t - t_p/RC)}\right]$$

* Response of low pass RC ckt for square wave i/p:-



output:-



→ waveform which maintains it self at one constant level. V for a time T_1 and at other constant level 'v' for a time T_2 and which is of a period $T = T_1 + T_2$ is called square wave.

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INSTITUTE OF ENGINEERING & TECHNOLOGY

(Approved by AICTE & Affiliated to JNTU)

Vinobha Nagar, Ibrahimpatnam, Ranga Reddy Dist – 501 506, Telangana, INDIA.
Ph: 08414-222799, 9177607659. Fax: 08414-222399
E-mail:info@siddhartha.ac.in; www.siddhartha.ac.in

NATIONAL BOARD of ACCREDITATION

College Code -TP

Date: 05/09/2020.

Financial Support Request Letter

1. Name of the staff member : Dr. S. Vijaya Mohan Rao
2. Designation : Professor
3. Department : CSE
4. Conference /publication/membership fee/workshop/fdp certificate details:
   Advanced Computing Applications in CSE Engineering.
   At. Vignan Institute of Technology & Science.
5. Date and duration of the program : 07-09-2020 to 11-09-2020.
6. Associating professional body/agency :
7. Financial supports particulars(Rs.) :
   i) Registration charges : 800/-
   ii) Travelling allowances :
   iii) Membership fee :
   iv) Other if any :

Date :

S. Vijaya Mohan Rao
signature of the staff member

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1. Recommendations of the HoD : Recommended
2. Recommendations of the IQAC : Recommended
3. Recommendations of the Principal :

Sanctioned/Not Sanctioned

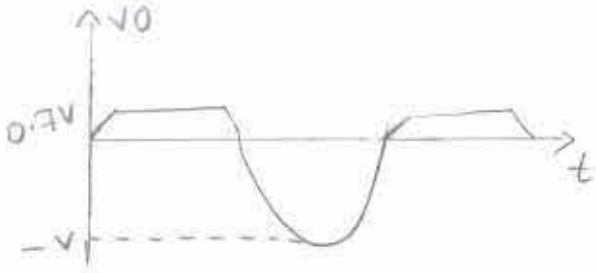
Account department

Accountant :

Date :

SIDDHARTHA INSTITUTE OF ENGINEERING & TECHNOLOGY
IQAC COORDINATOR
Vinobha Nagar, Ibrahimpatnam R. R. Dist. 501506.

output wave form



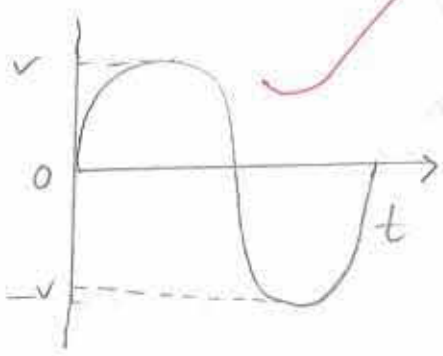
→ during the positive half cycle of AC signal diode is forward bias.

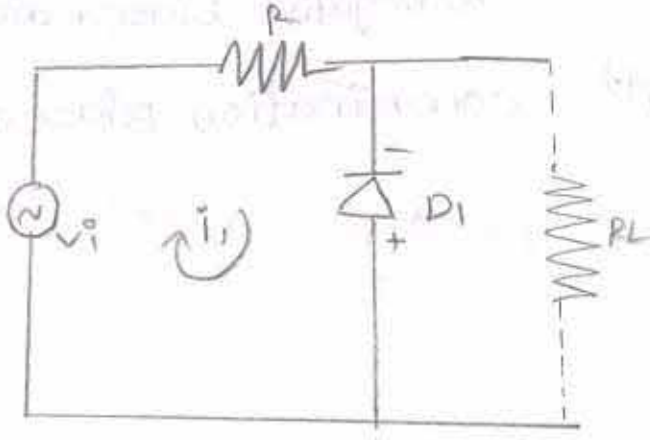
→ during the negative half cycle of AC signal diode is reverses bias.

→ current pass Through the diode. A is After 0.7V.

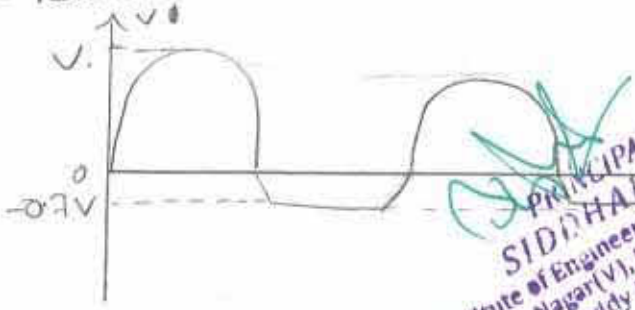
→ The output is same as the i/p signal.

* negative diode clipper:-





output wave-form:



→ during the positive half cycle of AC signal diode is reverse bias.

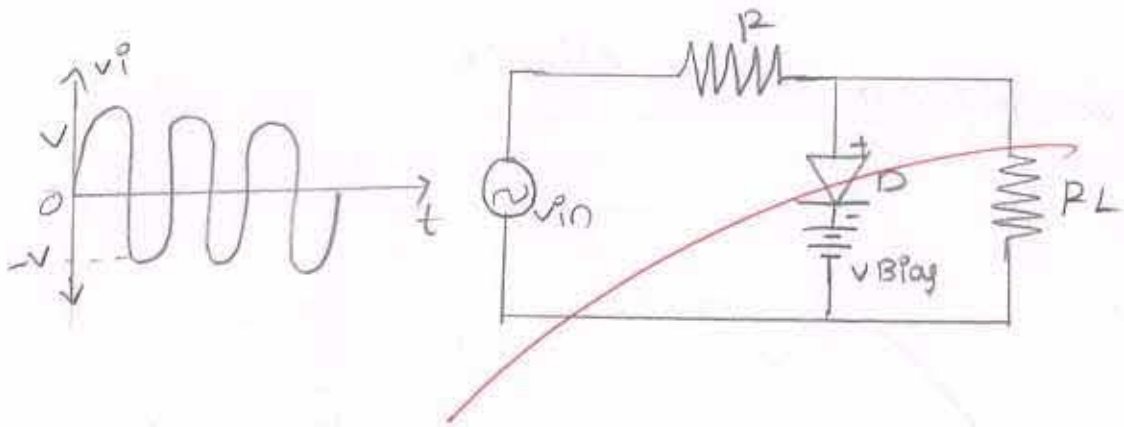
→ during the negative half cycle of AC signal diode is forward bias.

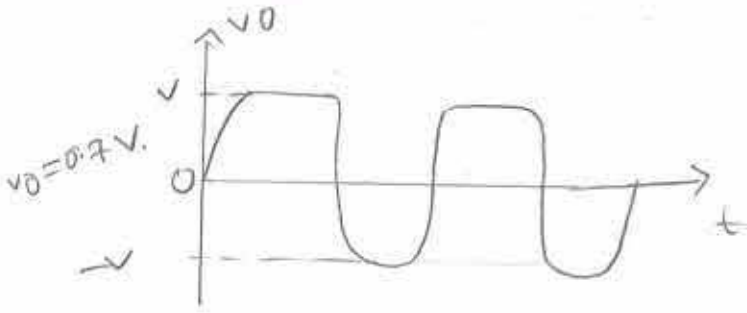
→ current pass through the diode after 0.7V

→ The output is same as input signal.

* Biased diode clipper

(a) positive diode clipper:-





→ during the positive half cycle of AC signal is forward bias.

→ V_{Bias} voltage, It acting as open circuit.

→ 0.7V as 0.7V is cut in voltage of silicon diode.

→ The output voltage will be equal to the cut in The voltage diode pulse voltage drop across V_{Bias}.

→ i/p voltage always greater than the bias voltage.

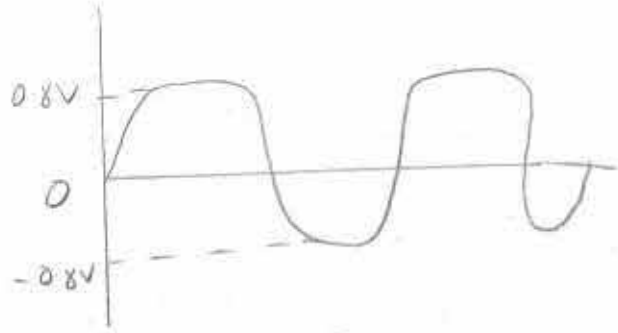
Ex:- $0.7V + 5V = 5.7V = V_0$

If $V_{Bias} = 2V$. $V_i = 3V$

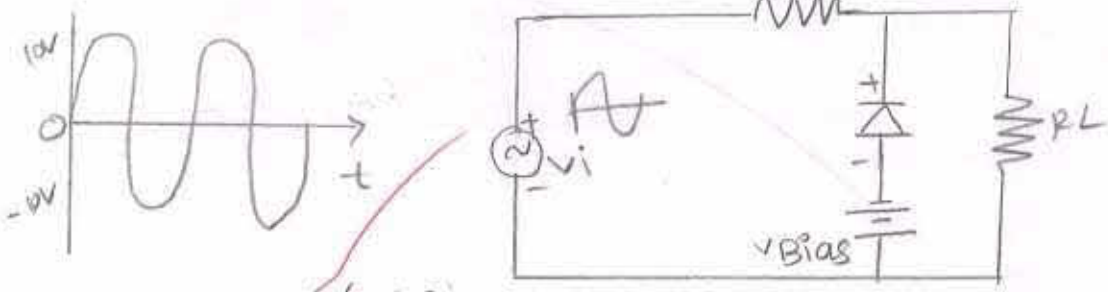
$V_0 = 0.7V + V_{Bias}$

$V_0 = 0.7V + 2V$

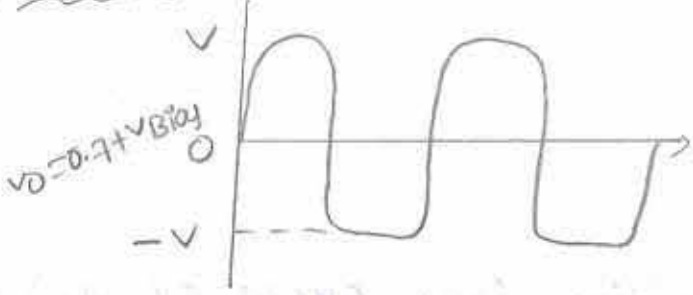
$V_0 = 0.8V$



* negative biased diode clipper:-



output wave form:-



→ during the negative half cycle AC signal diode is foward bias.

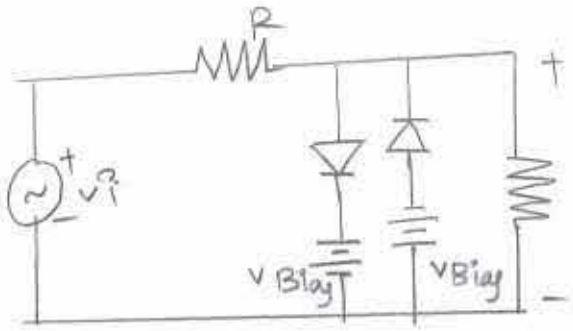
→ during the positive half cycle. AC signal diode is reverse bias.

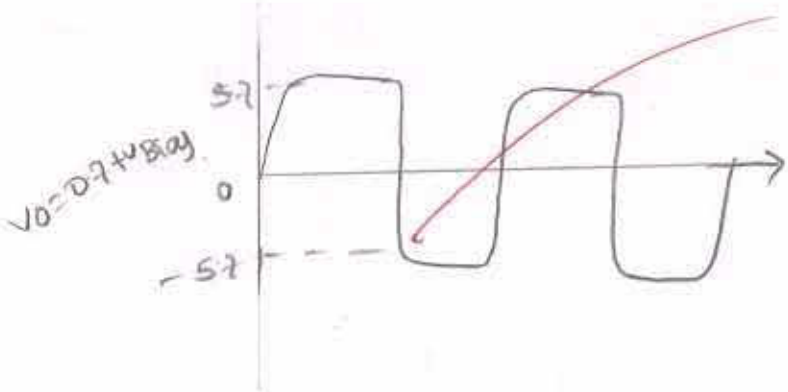
After from the 0.7V cut in voltage across the drop

→ Vout is equal to input signal.

→ It acting as a short ckt.

* combination biased Diode clipper:-





$V_{in} = 10V$, $V_{B_1} = 5V$. $V_{B_2} = 5V$

$V_o = 0.7 + V_{Biay}$

$V_o = 0.7 + 5V$

$V_o = 5.7V$

$V_o = 5.7V$

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P. Ramya

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PDC – II

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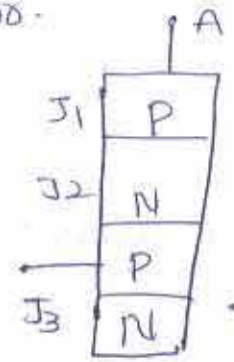
1) explain in detailed about silicon controlled switch ckt.

→ silicon controlled switch is a basic electronic device.

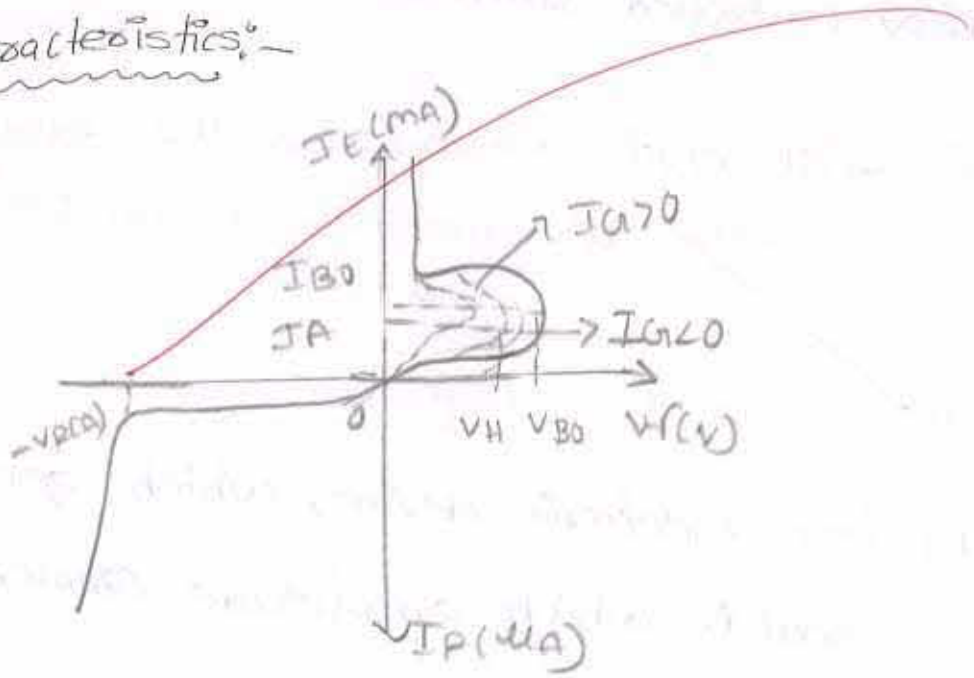
→ It is constructed by using P & N type semicondu -ctor.



→ It is a two terminal device. (anode (-) cathode (+))

→ It is having three junctions. J_1 J_2 and J_3.

output characteristics:-



I_H → Holding current

I_{BO} → break over current

V_{BO} → Break over voltage

V_H → Holding voltage.

logic symbol

Applications:

→ rectifiers.

→ Motor controllers.

→ power regulators

→ relays.

→ when transistor without applying the Gate i/p the construction of the PN junction diode is working as a normal diode.

→ If IG<0 it is reverse bias and it allows. The flow of current through P+N type

→ silicon controlled switch is used in motor controlled.

(2) explain with neat diagram for the following time base Generator. (a) miller sweep. (b) Boot strap sweep.

* miller sweep time base Generator:-

→ It is a electronic device, which generates time base signal in which amplitude. varies with respect to time.

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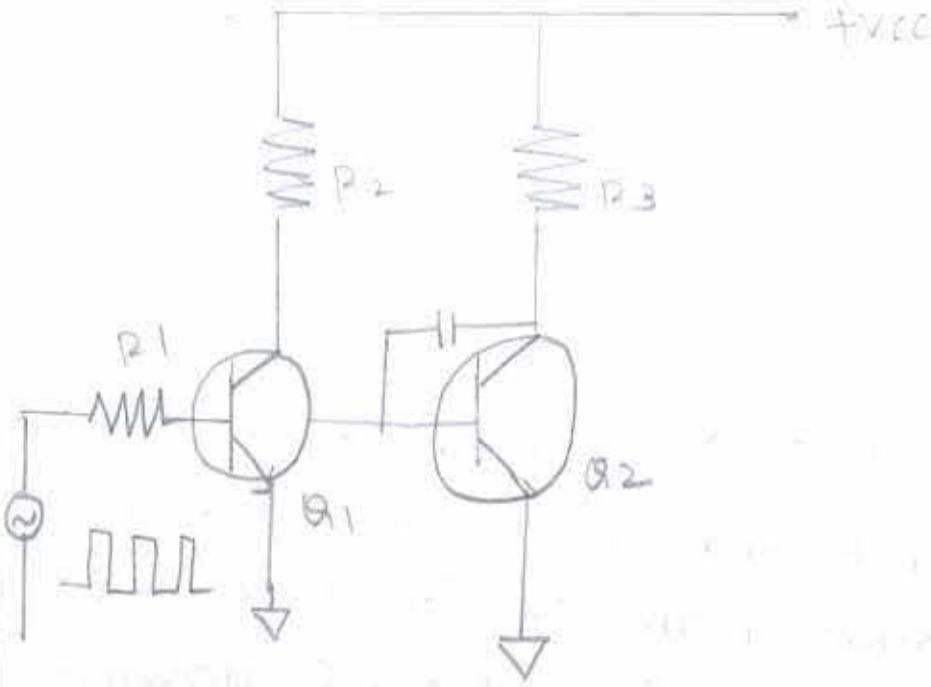
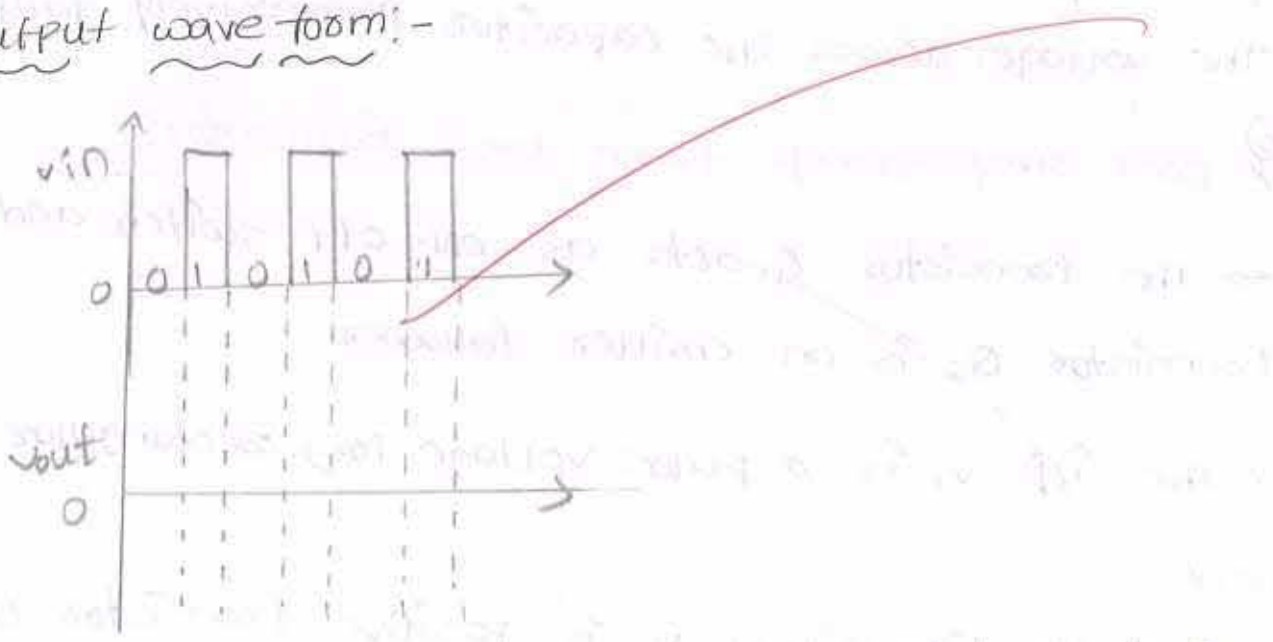


output waveform:-



→ Transistor Q_1 acts as ON-off switch and Q_2 is high gain Amplifier.

→ The i/p V_i is pulse or rectangular voltage.

→ When i/p signal is V_i is positive Q_1 become ON goes into the saturation region the potential at point

V_A becomes zero

$V_A = V_{CE} = 0$

→ Transistor Q_2 remains off since it cannot get the necessary base drive point 'B' potential. is V_{CC}. voltage across the capacitor.

→ Q_1 off and potential of 'A' going up Q_2 become. ON the potential of 'B' tends to decreases to zero but ~~become~~ because of the capacitor is V_A. gradually is increases V_B is gradually is decreases. The voltage across the capacitor progressively fall.

(b) * Boot strap sweep time base Generator:-

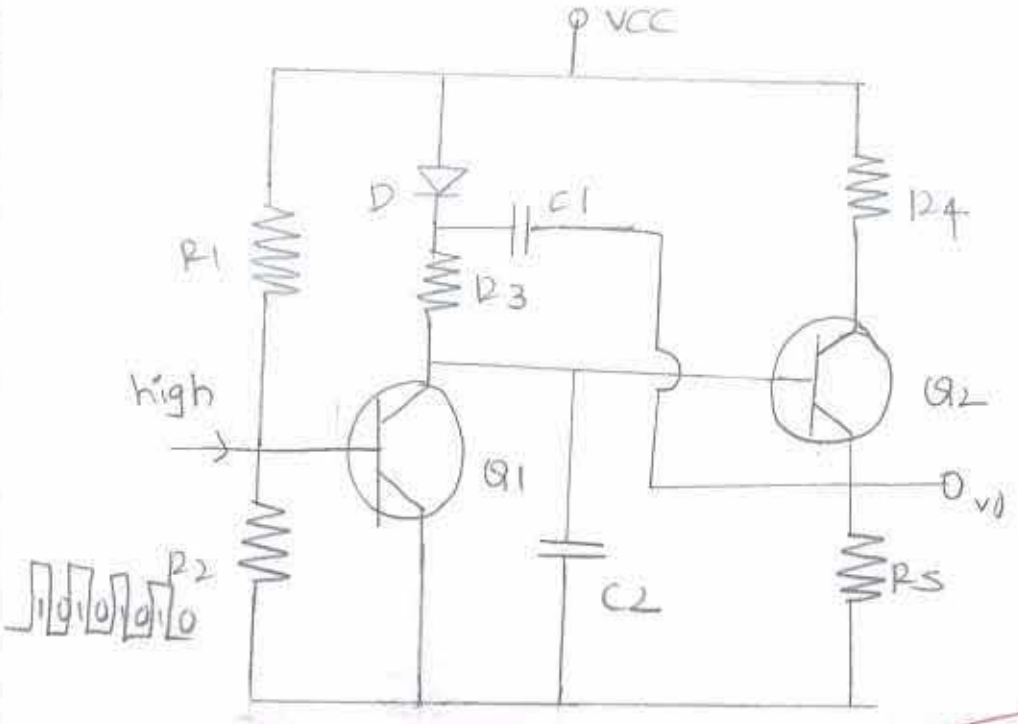
→ The transistor Q_1 acts as ON-off switch and the transistor Q_2 is an emitter followed.

→ The i/p V_1 is a pulse voltage (or) rectangular wave.

→ when the i/p signal V_1 is positive transistor Q_1 becomes ON goes into saturation.

∴ potential point A $V_A = V_{CE(sat)}$

→ The emitter of Q_2 is coupled to [illegible] of Q_1 Through the capacitor is C_B

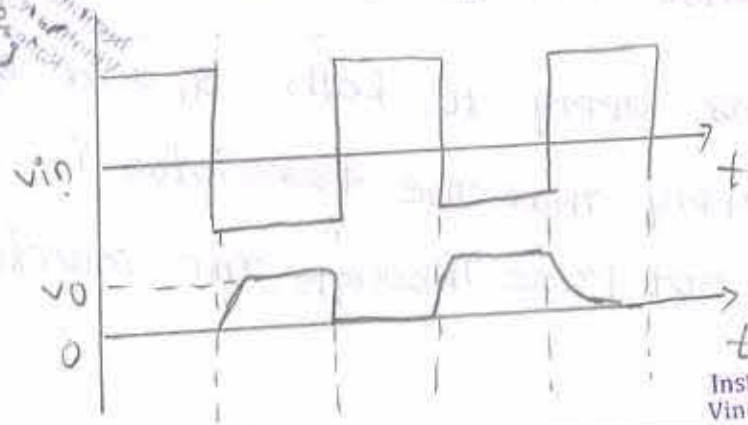


→ point 'B' become negative. w.r.to Vcc diode. D' readily conducts with the result the potential

$V_B \approx V_{CC}$

→ I/P V_i goes negative. Q_1 become off the potential. If A rises the increases of voltage at 'A' is transmitted to B' Through Q2 capacitor C3 This is the poincple of boot strap

output wave



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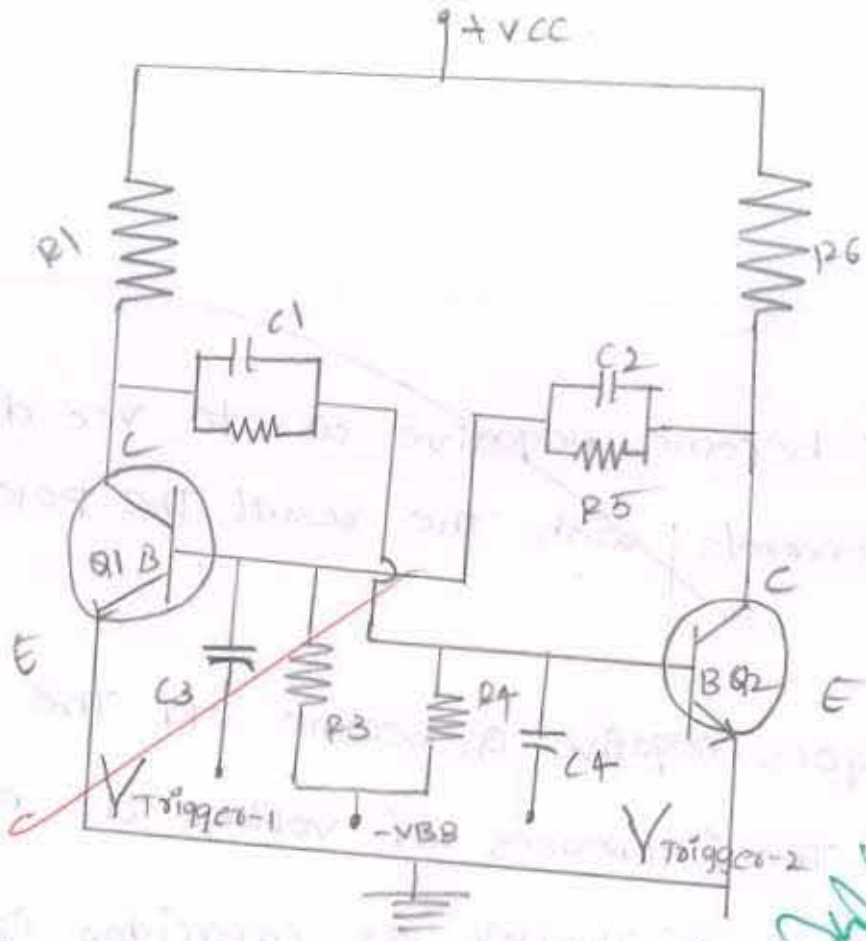
(3) draw and explain the working principle of bistable multivibrators

Bistable multivibrators:-

It is a stable at logic '0' and logic '1' state.

Design and analysis of Bistable multivibrators:-



→ It is a vibrator is two stage

→ multivibrator are used design the flop.

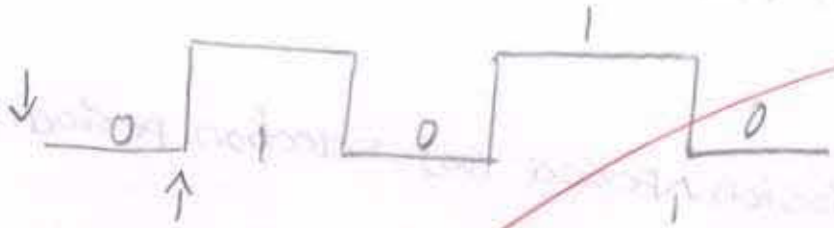
→ when Vmax. apply to both Q_1 and Q_2 transistor when we apply that the transistor is off so the current does not pass through the collector to Base, to emitter.

→ when the transistor is ON it acts as a saturation region and the voltage is V_{max} ↑

→ when the transistor is off it acts as cut of region so the voltage is V_{min} ↓

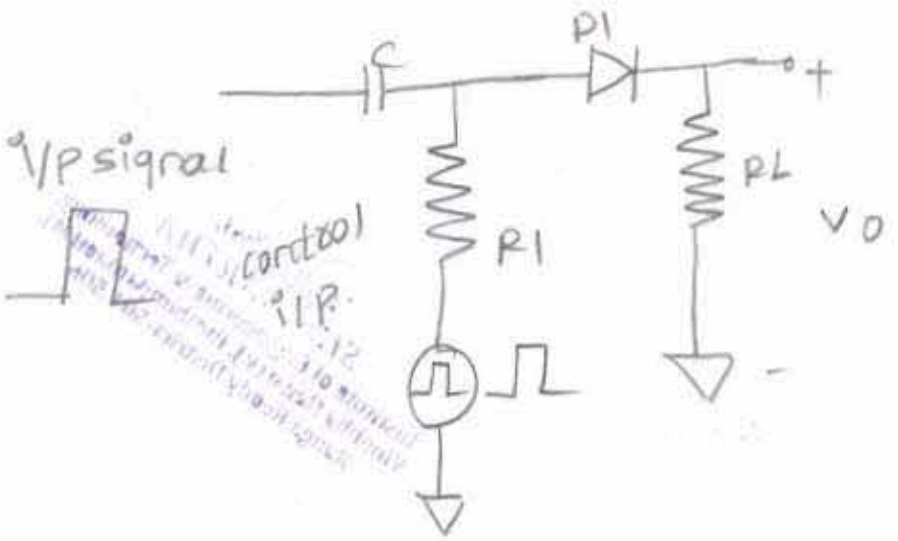
→ when two transistors are off the current passes through $R_1 C_1 P_2 P_5$ and C_2 so that the capacitors are charged.

output waveform:-



4) explain the operation of uni direction and Bi-direction sampling gate.

* uni-directional sampling gate:-



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→ control input decides the PN junction diode is open ckt. (or) short ckt.

→ If the control I/P signal is low PN junction does not connects.

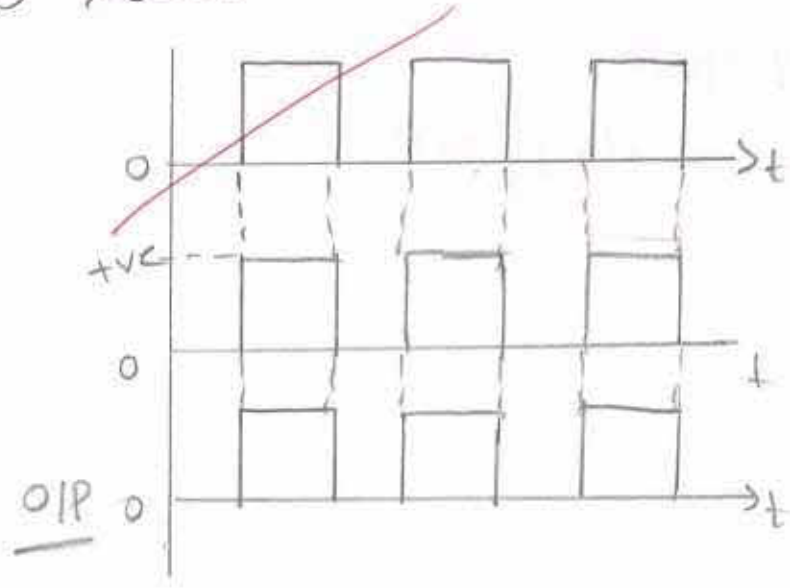
→ anode is very less component to cathode then the diode act as a reverse bias.

→ Then the o/p is zero of open ckt ($V_0 = zero$)

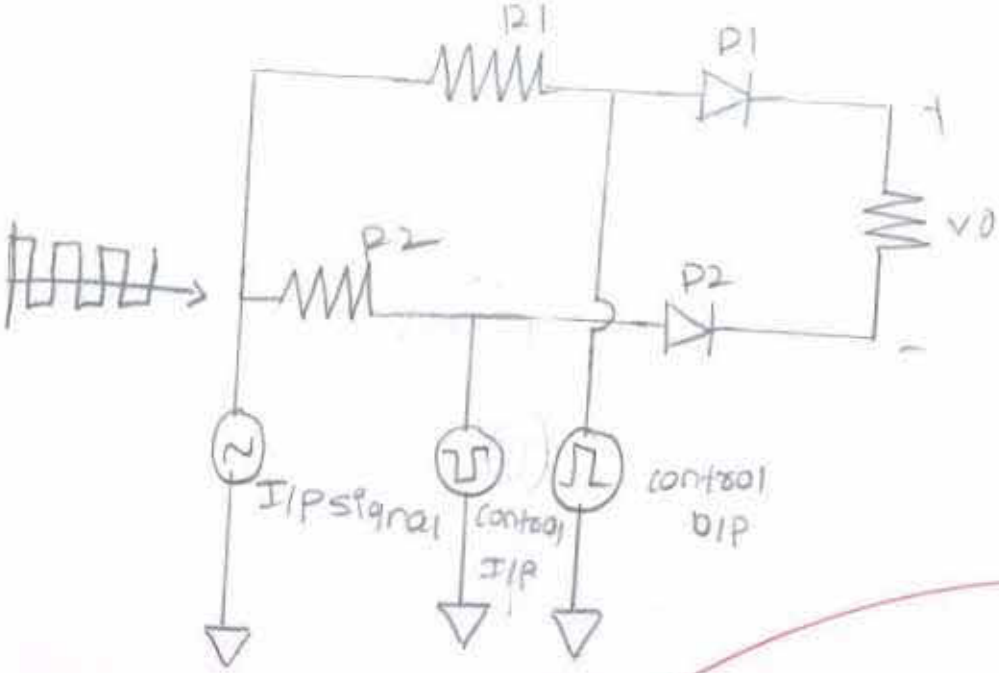
→ when the I/P signal is high then Tq acts. and the diode is open ckt. Then the output is maximum [$V_0 = max$].

→ Tq is transmission period (or) selection period.

output waveform:-



* Bi-directional sampling Gate:-



→ It produces the +ve waveforms and -ve waveforms are continuously.

→ during the -ve low control I/P forward bias D_1 is off D_2 is ON.

→ during the +ve high control I/P is forward bias D_1 (Diode) is ON. and D_2 is off & it pass through the resistance.

→ Bi-directional sampling gate is both (+ve) and (-ve) half cycle of the I/P signal.

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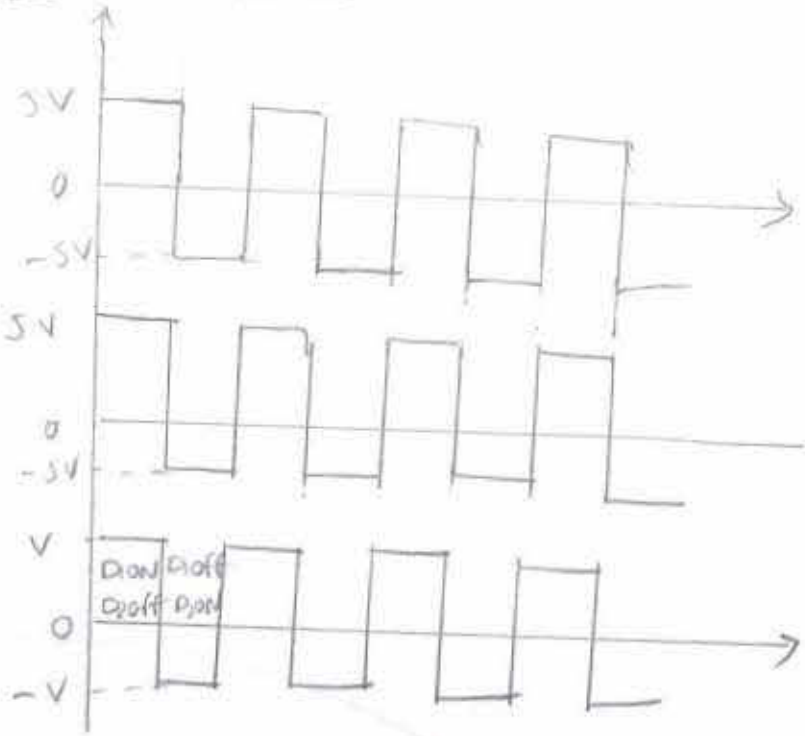
output wave forms:-



5) realize and The AND and OR Gate using diode transistors.

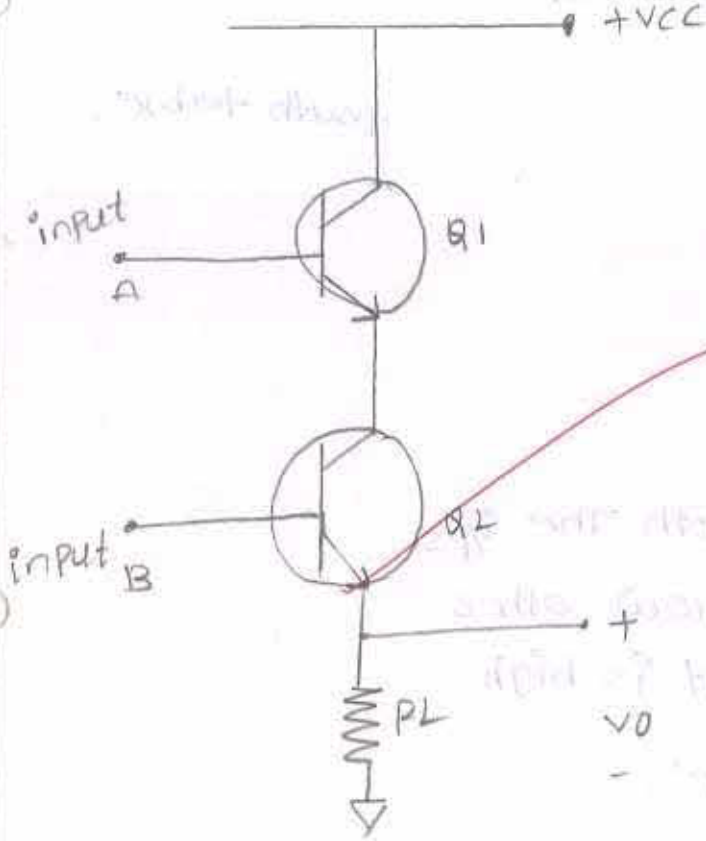
Truth table

Input		output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

AND gate is logic gate with multiple numbers of i/p's but only one output The output of AND gate is logic '1' (or) high only. If all The inputs are high else The output is zero.

→ 2 input AND gate using diodes The inputs are indicated by 'A' and B and 'y' indicates The output.

* Implementation of AND gate using transistor:-



$C = A \cdot B$

Truth table.

A	B	C=A·B
0	0	0
0	1	0
1	0	0
1	1	1

→ If A=0, B=0 both Q_1 & Q_2 are off. It is open circuit current does not allow Q_1 & Q_2 The output voltage is 0 The transistor acts as a cut off region.

→ If A=0, B=1 when we apply +Vcc current pass Thro -ugh Q_1 and current does not allows The current Q_2

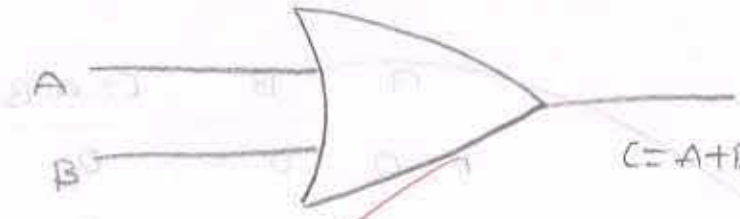
→ for A=1, B=0 Q_1 is ON current passes Through Q_1 & Q_2 is off output Vo is 0'

→ for A=1, B=1 both Q_1 & Q_2 transistor are 'ON' current passes from V_{CC} to load resistance RL and passes Through ground output voltage 'Vo' is '1'

Implementation of OR gate using diode:-

→ OR gate is an electronic device it can perform OR - operation b/w given operands.

logic symbol:-

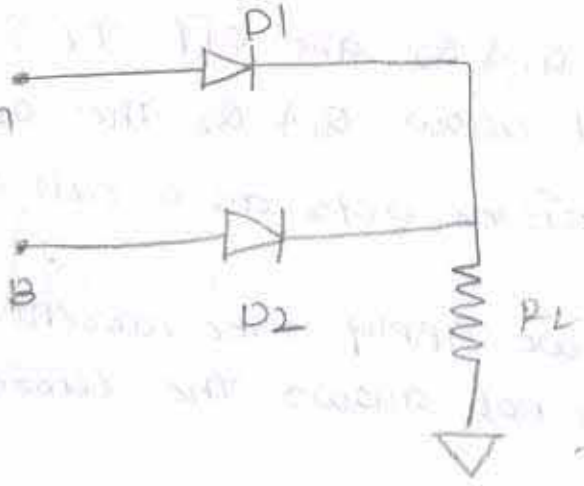


truth table.

A	B	C=A+B
0	0	0
0	1	1
1	0	1
1	1	0

→ In OR Gate operation both The i/p's are low Then The o/p is low other -wise, in all cases output is high

Implementation using diode:-



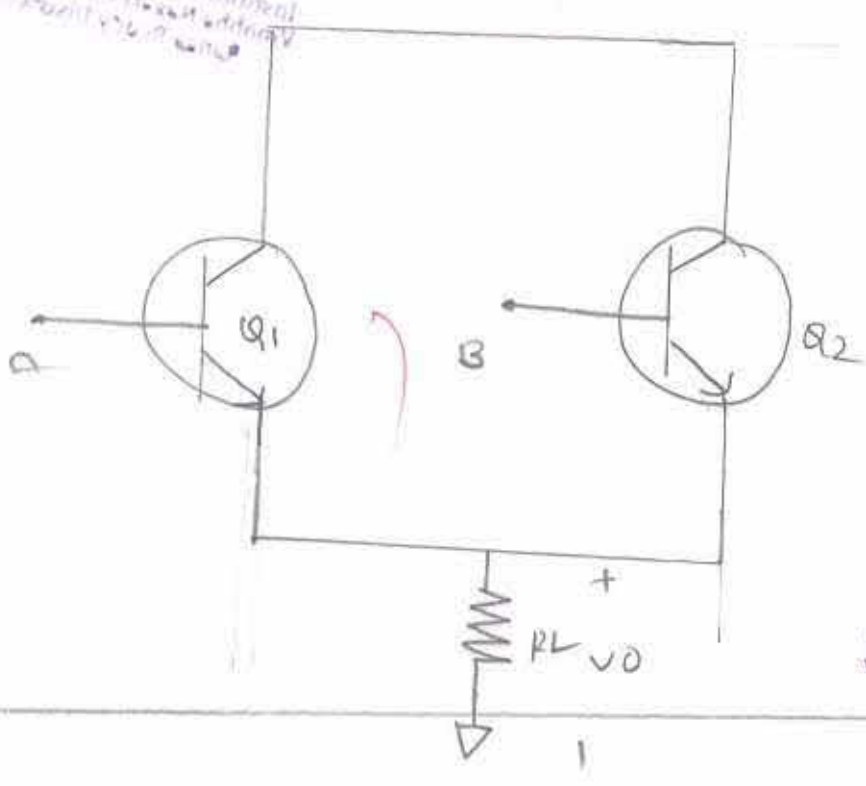
→ If we give input A=0, B=0 PN junction diode is open circuit there is no current is passes Through D_1 and D_2 The o/p voltage v_o is '0'

→ If A=0, B=1 · Q_1 transistor is off But Q_2 transis -tor is ON and passes Through load resistance R_L o/p voltage v_o is 1

→ If A=1, B=0 passes Through load resistance R_L and o/p voltage v_o is '1'

→ If we give A=1, B=1 Through passes both The diodes D_1 & D_2 is ON Then The o/p voltage v_o '1' & current passes Through load resistance R_L and go to The ground.

* Implementation of OR gate using transistor;-



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→ If A=0, B=0 transistor Q_1 & Q_2 is off output voltage V_o is '0' A=0, B=0. current is open circuit

→ A=0, B=1. Q_1 is off and Q_2 is ON current passes Through Q_2 V_o is '1'

→ If A=1, B=0 current pass through Q_1 & Q_2 is ON. Q_2 is off output voltage. V_o is '1'

→ If A=1, B=1 current passes Through Q_1 & Q_2 both The transistor are 'ON' Then The output voltage is V_o is '0'

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(Approved by AICTE & Affiliated to JNTU)

Vinobha Nagar, Ibrahimpatnam, Ranga Reddy Dist – 501 506, Telangana, INDIA.
Ph: 08414-222799, 9177607659. Fax: 08414-222399
E-mail:info@siddhartha.ac.in; www.siddhartha.ac.in

NATIONAL BOARD OF ACCREDITATION

College Code -TP

Date: 16/11/2019

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1. Name of the staff member : Uday Bhaskar Nalla
2. Designation : Assistant professor
3. Department : Civil
4. Conference /publication/membership fee/workshop/fdp certificate details:
   Auto desk auto CAD
   at MLR Institute of Technology
5. Date and duration of the program : 18/11/2019 to 22/11/2019
6. Associating professional body/agency : _____
7. Financial supports particulars(Rs.) : _____
   i) Registration charges : 0800/-
   ii) Travelling allowances : _____
   iii) Membership fee : _____
   iv) Other if any : _____

Date :

signature of the staff member

1. Recommendations of the HoD : Recommended - Yes
2. Recommendations of the IQAC : Recommended
3. Recommendations of the Principal : Recommended

Sanctioned/Not Sanctioned

Account department

Accountant :

Date :

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IQAC COORDINATOR
Vinobha Nagar, Ibrahimpatnam, R.R Dist., 501506.

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Department:	EC E		
Course Outcome Attainment - Internal Assessments			
Name of the faculty :	T KRISHNARJUNA RAO	Academic Year:	2018-2019
Branch & Section:	A&B	Exam:	PDC INTERNAL-I
Course:	B.TECH	Semester :	II-SEM

Sl.No	Roll Number	Question No.				Objective	Assignment
		1	2	3	4		
Maximum Marks		5	5	5	5	10	5
1	15TP1A04A1	4		4		7	0
2	16TP1A0410	4	4			7	0
3	16TP1A0428	5	5			10	5
4	16TP1A0434	3	4			3	5
5	16TP1A0447	4	4			8	0
6	17TP1A0401	5			5	10	5
7	17TP1A0402	5		5		10	5
8	17TP1A0403	5	5			10	5
9	17TP1A0404		5	5		10	5
10	17TP1A0405			5	5	10	5
11	17TP1A0406		5		5	10	5
12	17TP1A0407			5	5	10	5
13	17TP1A0408		5		5	10	5
14	17TP1A0409			5	5	10	5
15	17TP1A0411	5	5			10	5
16	17TP1A0412	5			5	10	5

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17	17TP1A0413	5			5	10	5
18	17TP1A0414	5	5			10	5
19	17TP1A0416	4	4			8	5
20	17TP1A0417			5	5	9	5
21	17TP1A0418		4		4	9	5
22	17TP1A0419		5		5	10	5
23	17TP1A0420	5		5		10	5
24	17TP1A0421	5	5			10	5
25	17TP1A0423		5		5	10	5
26	17TP1A0424		5		5	10	5
27	17TP1A0425	4		4		9	5
28	17TP1A0427			5	5	10	5
29	17TP1A0428	5	5			10	5
30	17TP1A0430		5		5	10	5
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40	17TP1A0441	5			5	9	5

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42	17TP1A0443		5		5	10	5
43	17TP1A0444			5	5	10	5
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63	17TP1A0466	5	5			10	5
64	17TP1A0467		5	5		10	5

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65	17TP1A0469		5	5		10	5
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77	17TP1A0484	5	5			9	5
78	17TP1A0485			5	4	10	5
79	17UR1A0401	5			5	10	5
80	17UR1A0404	5			5	10	5
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84	18TP5A0405	5		3		9	3
85	18TP5A0407	3	4			8	4
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87	18TP5A0409	4	4			10	4
88	18TP5A0410	4	4			5	2

89	18TP5A0411	3			5	8	4
90	18TP5A0412	4		4		7	4
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92	18TP5A0414	5		5		10	4
93	18TP5A0415	4		5		9	4
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103	18TP5A0425	4			5	8	4
104	18TP5A0426			4	5	7	4
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110	18TP5A0432			5	5	9	4
111	18TP5A0433			4	4	10	4
112	18TP5A0435			4	4	4	4

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113	18TP5A0436			4	5	10	5
114	18TP5A0437	5	5			9	5
115	18TP5A0438	4	4			8	5
116	18TP5A0439		5	5		7	5
Total Score		323	257	217	260	1503	525
Total Number of studets		71	58	48	55	116	116
Average Score		4.6	4.7	4.6	4.8	9.2	4.5

No. of students > target score	71	58	48	55	114	111
% of students > target score	100	100	100	100	98.2	95.6

Course Outcome Mapping with each Question

Course outcome - 1	Y	Y			Y	Y
Course outcome - 2			Y	Y	Y	Y
Course outcome - 3					Y	Y
Course outcome - 4						
Course outcome - 5						

Course Outcome Attainment based on Exam Questions in terms of percentage of total students when mapped to each question

Course outcome - 1	100	100			99	95.6
Course outcome - 2			100	100	99	95.6
Course outcome - 3					99	95.6
Course outcome - 4						
Course outcome - 5						

Attainment for all components	Subjective	Objective	Assignment	Overall	Attainment Level
Course outcome - 1	100	99	95.6	98.2	3
Course outcome - 2	100	99	95.6	98.2	3
Course outcome - 3		99	95.6	97.3	3
Course outcome - 4					
Course outcome - 5					
Overall Course attainment as average attainment level					3

Sl.No	Roll Number	Target %= 50%					
		Question No.				Obj1	A1
Maximum Marks		1	2	3	4	5	5
			Target score	2.5	2.5	2.5	2.5
1.	15TP1A04A1	1		1		1	0
2.	16TP1A0410	1	1			1	0
3.	16TP1A0428	1	1			1	1
4.	16TP1A0434	1	1			0	1
5.	16TP1A0447	1	1			1	0
6.	17TP1A0401	1			1	1	1
7.	17TP1A0402	1		1		1	1
8.	17TP1A0403	1	1			1	1
9.	17TP1A0404		1	1		1	1
10.	17TP1A0405			1	1	1	1

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11.	17TP1A0406		1		1	1	1
12.	17TP1A0407			1	1	1	1
13.	17TP1A0408		1		1	1	1
14.	17TP1A0409			1	1	1	1
15.	17TP1A0411	1	1			1	1
16.	17TP1A0412	1			1	1	1
17.	17TP1A0413	1			1	1	1
18.	17TP1A0414	1	1			1	1
19.	17TP1A0416	1	1			1	1
20.	17TP1A0417			1	1	1	1
21.	17TP1A0418		1		1	1	1
22.	17TP1A0419		1		1	1	1
23.	17TP1A0420	1		1		1	1
24.	17TP1A0421	1	1			1	1
25.	17TP1A0423		1		1	1	1
26.	17TP1A0424		1		1	1	1
27.	17TP1A0425	1		1		1	1
28.	17TP1A0427			1	1	1	1
29.	17TP1A0428	1	1			1	1
30.	17TP1A0430		1		1	1	1
31.	17TP1A0431		1		1	1	1
32.	17TP1A0432	1	1			1	1
33.	17TP1A0433	1			1	1	1
34.	17TP1A0434	1	1			1	1

35.	17TP1A0435	1	1			1	1
36.	17TP1A0436	1			1	1	1
37.	17TP1A0437	1			1	1	1
38.	17TP1A0438		1		1	1	1
39.	17TP1A0439	1			1	1	1
40.	17TP1A0441	1			1	1	1
41.	17TP1A0442	1	1			1	1
42.	17TP1A0443		1		1	1	1
43.	17TP1A0444			1	1	1	1
44.	17TP1A0445			1	1	1	1
45.	17TP1A0446	1	1			1	1
46.	17TP1A0447	1	1			1	1
47.	17TP1A0448		1		1	1	1
48.	17TP1A0449	1			1	1	1
49.	17TP1A0450	1	1			1	1
50.	17TP1A0451	1		1		1	1
51.	17TP1A0452	1	1			1	1
52.	17TP1A0453	1		1		1	1
53.	17TP1A0454	1	1			1	1
54.	17TP1A0455	1	1			1	1
55.	17TP1A0457			1	1	1	1
56.	17TP1A0458	1	1			1	1
57.	17TP1A0459		1		1	1	1
58.	17TP1A0460		1	1		1	1

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59.	17TP1A0461	1			1	1	1
60.	17TP1A0462	1			1	1	1
61.	17TP1A0464	1	1			1	1
62.	17TP1A0465	1		1		1	1
63.	17TP1A0466	1	1			1	1
64.	17TP1A0467		1	1		1	1
65.	17TP1A0469		1	1		1	1
66.	17TP1A0472	1		1		1	1
67.	17TP1A0473			1	1	1	1
68.	17TP1A0474		1	1		1	1
69.	17TP1A0475	1	1			1	1
70.	17TP1A0476		1		1	1	1
71.	17TP1A0477	1	1			1	1
72.	17TP1A0479		1	1		1	1
73.	17TP1A0480	1	1			1	1
74.	17TP1A0481		1	1		1	1
75.	17TP1A0482	1	1			1	1
76.	17TP1A0483			1	1	1	1
77.	17TP1A0484	1	1			1	1
78.	17TP1A0485			1	1	1	1
79.	17UR1A0401	1			1	1	1
80.	17UR1A0404	1			1	1	1
81.	18TP5A0401	1			1	1	0
82.	18TP5A0402	1				1	1

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83.	18TP5A0404	1			1	1	1
84.	18TP5A0405	1		1		1	1
85.	18TP5A0407	1	1			1	1
86.	18TP5A0408	1	1			1	1
87.	18TP5A0409	1	1			1	1
88.	18TP5A0410	1	1			1	0
89.	18TP5A0411	1			1	1	1
90.	18TP5A0412	1		1		1	1
91.	18TP5A0413	1		1		1	1
92.	18TP5A0414	1		1		1	1
93.	18TP5A0415	1		1		1	1
94.	18TP5A0416			1	1	1	1
95.	18TP5A0417	1		1		1	1
96.	18TP5A0418	1		1		1	1
97.	18TP5A0419			1	1	1	1
98.	18TP5A0420			1	1	1	1
99.	18TP5A0421	1	1			1	1
100.	18TP5A0422	1			1	1	1
101.	18TP5A0423	1		1		1	1
102.	18TP5A0424			1	1	1	1
103.	18TP5A0425	1			1	1	1
104.	18TP5A0426			1	1	1	1
105.	18TP5A0427			1	1	1	1
106.	18TP5A0428		1		1	1	1

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107.	18TP5A0429			1	1	1	1
108.	18TP5A0430			1	1	1	1
109.	18TP5A0431	1		1		1	1
110.	18TP5A0432			1	1	1	1
111.	18TP5A0433			1	1	1	1
112.	18TP5A0435			1	1	0	1
113.	18TP5A0436			1	1	1	1
114.	18TP5A0437	1	1			1	1
115.	18TP5A0438	1	1			1	1
116.	18TP5A0439		1	1		1	1
Total Students more than target score Count		68	55	47	54	112	111
% students greater than target		68	55				

Attainment Level	Overall attainment
1	>=60%
2	>=70%
3	>=80%

SIDDHARTHA INSTITUTE OF ENGINEERING & TECHNOLOGY			
Department:			
Overall Course Outcome Attainment as per University result			
Name of the faculty :	T KRISHNARJUNA RAO	Academic Year:	2018-2019
Branch & Section:	ECE	Exam:	PDC INTERNAL -1
Course:		Semester:	II

S. No	REG. NO	TOTAL Max score: 75
1.	15TP1A04A1	15
2.	16TP1A0410	24
3.	16TP1A028	44
4.	16TP1A0434	21
5.	16TP1A0447	19
6.	17TP1A0401	44
7.	17TP1A0402	21
8.	17TP1A0403	44
9.	17TP1A0404	44
10.	17TP1A0405	44
11.	17TP1A0406	44
12.	17TP1A0407	44
13.	17TP1A0408	44
14.	17TP1A0409	44
15.	17TP1A0411	44
16.	17TP1A0412	44
17.	17TP1A0413	44
18.	17TP1A0414	44
19.	17TP1A0416	21

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20.	17TP1A0417	44
21.	17TP1A0418	21
22.	17TP1A0419	19
23.	17TP1A0420	44
24.	17TP1A0421	37
25.	17TP1A0423	21
26.	17TP1A0424	21
27.	17TP1A0425	19
28.	17TP1A0427	44
29.	17TP1A0428	44
30.	17TP1A0430	44
31.	17TP1A0431	44
32.	17TP1A0432	21
33.	17TP1A0433	44
34.	17TP1A0434	44
35.	17TP1A0435	44
36.	17TP1A0436	44
37.	17TP1A0437	44
38.	17TP1A0438	44
39.	17TP1A0439	44
40.	17TP1A0441	21
41.	17TP1A0442	44
42.	17TP1A0443	21

43.	17TP1A0444	44
44.	17TP1A0445	37
45.	17TP1A0446	44
46.	17TP1A0447	44
47.	17TP1A0448	44
48.	17TP1A0449	44
49.	17TP1A0450	44
50.	17TP1A0451	44
51.	17TP1A0452	44
52.	17TP1A0453	44
53.	17TP1A0454	44
54.	17TP1A0455	44
55.	17TP1A0457	44
56.	17TP1A0458	44
57.	17TP1A0459	44
58.	17TP1A0460	21
59.	17TP1A0461	44
60.	17TP1A0462	44
61.	17TP1A0464	44
62.	17TP1A0465	44
63.	17TP1A0466	44
64.	17TP1A0467	44
65.	17TP1A0469	44

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66.	17TP1A0472	21
67.	17TP1A0473	37
68.	17TP1A0474	21
69.	17TP1A0475	37
70.	17TP1A0476	21
71.	17TP1A0477	44
72.	17TP1A0479	37
73.	17TP1A0480	44
74.	17TP1A0481	37
75.	17TP1A0482	44
76.	17TP1A0483	37
77.	17TP1A0484	44
78.	17TP1A0485	44
79.	17UR1A0401	44
80.	17UR1A0404	59
81.	18TP5A0402	37
82.	18TP5A0404	37
83.	18TP5A0405	21
84.	18TP5A0407	Ab
85.	18TP5A0408	44
86.	18TP5A0409	44
87.	18TP5A0410	21
88.	18TP5A0411	Ab

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BEYOND THE SYLLABUS

What are some of the differences between CMOS and TTL signals and how do they compare?

Solution

Characteristics of CMOS logic:

- Dissipates low power: The power dissipation is dependent on the power supply voltage, frequency, output load, and input rise time. At 1 MHz and 50 pF load, the power dissipation is typically 10 nW per gate.
- Short propagation delays: Depending on the power supply, the propagation delays are usually around 25 nS to 50 nS.
- Rise and fall times are controlled: The rise and falls are usually ramps instead of step functions, and they are 20 - 40% longer than the propagation delays.
- Noise immunity approaches 50% or 45% of the full logic swing.
- Levels of the logic signal will be essentially equal to the power supplied since the input impedance is so high.
- Voltage levels range from 0 to VDD where VDD is the supply voltage. A low level is anywhere between 0 and 1/3 VDD while a high level is between 2/3 VDD and VDD.

Characteristics of TTL logic:

- Power dissipation is usually 10 mW per gate.
- Propagation delays are 10 nS when driving a 15 pF/400 ohm load.
- Voltage levels range from 0 to Vcc where Vcc is typically 4.75V - 5.25V. Voltage range 0V - 0.8V creates logic level 0. Voltage range 2V - Vcc creates logic level 1.

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TEACHER FEEDBACK ON CURRICULUM

Name: J. Nagaraju	**Section:** A
Subject: EMTL	**Year:** III
Academic Year: 2019-20	**Semester:** I

Grade the degree to which the prescribed syllabus and curriculum augments their defined objectives with (a)High-3 (b)Moderate-2 (c)Low-1 (d)Poor-0

S.NO	CONTENT	GRADE
1.	Relevance of text books and reference books to the prescribed syllabus	3
2.	Whether the course content help student to acquire employment	3
3.	Extent the course is framed based in the needs of the follow on courses	2
4.	Whether any relevance between syllabus and course	3
5.	Does the course provide adequate hands on training	2
6.	Extent to which the curriculum requires modern books usage	2
7.	Whether the course content meet industrial requirement	3

COURSE NAME	GAPS IDENTIFIED
EMTL	Vector Analysis.

Suggestions if any: —

Signature

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STUDENT FEEDBACK

Year	III	Section	ECE-B
Academic year	2026-2027	Semester	I

Give grading to which the syllabus augments course in attaining their defined objectives with
(a) high-3 (b) moderate-2 (c) low-1 (d) poor-0

S.NO	Content	SUB-1	SUB-2	SUB-3	SUB-4	SUB-5	SUB-6
		MPMC	DCN	CG	BETA	COOS	CYS
1	Whether the syllabus of the course meets their objectives laid down?	3	3	3	3	3	3
2	Interaction between the students and Teacher.	3	3	3	3	3	3
3	Teacher's knowledge on the Subject.	3	3	3	3	3	3
4	How well the Teacher explained the Content?	3	3	2	3	3	3
5	Extent to which the syllabus augments theory with its practical application?	3	3	3	3	3	3
6	Does the syllabus meet expected learning values like life skills, human values, gender equality with social response?	3	3	3	3	2	3
7	Whether there is relevance between course and the credits offered.	3	3	3	3	3	3
8	Whether the elective offered in the curriculum is relevant to your technological aspects?	3	3	3	3	3	3
9	Extent to which the syllabus covers all courses that help for higher studies/job opportunities?	3	3	3	3	3	3
10	Does the curriculum train you on critical, logical problem-solving techniques?	3	3	3	2	3	3
11	Whether curriculum is providing basic knowledge of technologies related to other domains?	3	2	3	2	3	3
	Average	3	2.9	2.9	2.8	2.9	3

Any suggestions:

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STUDENT FEEDBACK

Year	III	Section	ECE-B
Academic year	2028 2029	Semester	I

Give grading to which the syllabus augments course in attaining their defined objectives with
(a) high-3 (b) moderate-2 (c) low-1 (d) poor-0

S.NO	Content	SUB-1	SUB-2	SUB-3	SUB-4	SUB-5	SUB-6
		MPMC	DCN	CG	BEFA	COOS	CYS
1	Whether the syllabus of the course meets their objectives laid down?	3	3	3	3	3	3
2	Interaction between the students and Teacher.	3	3	3	3	3	3
3	Teacher's knowledge on the Subject.	3	3	3	3	3	3
4	How well the Teacher explained the Content?	3	3	2	3	3	3
5	Extent to which the syllabus augments theory with its practical application?	3	3	3	3	3	3
6	Does the syllabus meet expected learning values like life skills, human values, gender equality with social response?	3	3	3	3	2	3
7	Whether there is relevance between course and the credits offered.	3	3	3	3	3	3
8	Whether the elective offered in the curriculum is relevant to your technological aspects?	3	3	3	3	3	3
9	Extent to which the syllabus covers all courses that help for higher studies/job opportunities?	3	3	3	3	3	3
10	Does the curriculum train you on critical, logical problem-solving techniques?	3	3	3	2	3	3
11	Whether curriculum is providing basic knowledge of technologies related to other domains?	3	2	3	2	3	3
	Average	3	2.9	2.9	2.8	2.9	3

Any suggestions:

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STUDENT FEEDBACK

Year	III	Section	ECE
Academic year	2021 – 2022	Semester	I

Give grading to which the syllabus augments course in attaining their defined objectives with
(a) high-3 (b) moderate-2 (c) low-1 (d) poor-0

S.NO	Content	SUB-1	SUB-2	SUB-3	SUB-4	SUB-5	SUB-6
		MPMC	DCN	CS	Befa	COOS	CYS
1	Whether the syllabus of the course meets their objectives laid down?	3	3	3	3	3	3
2	Interaction between the students and Teacher.	3	3	3	3	3	3
3	Teacher's knowledge on the Subject.	3	3	3	3	3	3
4	How well the Teacher explained the Content?	3	3	3	3	3	3
5	Extent to which the syllabus augments theory with its practical application?	3	3	3	3	3	3
6	Does the syllabus meet expected learning values like life skills, human values, gender equality with social response?	3	3	3	3	3	3
7	Whether there is relevance between course and the credits offered.	3	3	3	3	3	3
8	Whether the elective offered in the curriculum is relevant to your technological aspects?	2	3	3	2	3	3
9	Extent to which the syllabus covers all courses that help for higher studies/job opportunities?	3	3	3	3	3	3
10	Does the curriculum train you on critical, logical problem-solving techniques?	3	3	2	3	3	3
11	Whether curriculum is providing basic knowledge of technologies related to other domains?	3	3	3	3	3	3
	Average	2.9	3	2.9	2.9	3	3

Any suggestions:

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STUDENT FEEDBACK

Year	3	Section	ECE-B
Academic year	21-22	Semester	3-1

Give grading to which the syllabus augments course in attaining their defined objectives with (a) high-3 (b) moderate-2 (c) low-1 (d) poor-0

S.NO	Content	SUB-1	SUB-2	SUB-3	SUB-4	SUB-5	SUB-6
		PCN	EVS	BEEA	M&MC	CS	COOS
1	Whether the syllabus of the course meets their objectives laid down?	3	3	3	3	3	3
2	Interaction between the students and Teacher.	3	3	3	3	3	3
3	Teacher's knowledge on the Subject.	3	3	3	3	3	3
4	How well the Teacher explained the Content?	3	3	3	3	3	3
5	Extent to which the syllabus augments theory with its practical application?	3	3	3	2	3	3
6	Does the syllabus meet expected learning values like life skills, human values, gender equality with social response?	3	3	3	3	3	3
7	Whether there is relevance between course and the credits offered.	3	3	3	3	3	3
8	Whether the elective offered in the curriculum is relevant to your technological aspects?	3	3	3	3	3	3
9	Extent to which the syllabus covers all courses that help for higher studies/job opportunities?	3	3	3	3	3	3
10	Does the curriculum train you on critical, logical problem-solving techniques?	3	3	3	3	3	3
11	Whether curriculum is providing basic knowledge of technologies related to other domains?	3	3	3	3	3	3
	Average	3	3	3	2.8	3	3.0

Any suggestions:

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STUDENT FEEDBACK

Year	III	Section	ECE-B
Academic year	2021-2022	Semester	I

Give grading to which the syllabus augments course in attaining their defined objectives with
(a) high-3 (b) moderate-2 (c) low-1 (d) poor-0

S.NO	Content	SUB-1	SUB-2	SUB-3	SUB-4	SUB-5	SUB-6
		MPMC	DCN	COOS	BEFA	CS	CYS
1	Whether the syllabus of the course meets their objectives laid down?	3	3	3	3	3	3
2	Interaction between the students and Teacher.	3	3	3	3	3	3
3	Teacher's knowledge on the Subject.	3	3	3	3	3	3
4	How well the Teacher explained the Content?	3	3	2	3	2	3
5	Extent to which the syllabus augments theory with its practical application?	2	3	3	3	3	3
6	Does the syllabus meet expected learning values like life skills, human values, gender equality with social response?	3	3	3	3	3	3
7	Whether there is relevance between course and the credits offered.	3	3	3	3	3	3
8	Whether the elective offered in the curriculum is relevant to your technological aspects?	3	3	3	3	3	3
9	Extent to which the syllabus covers all courses that help for higher studies/job opportunities?	3	3	3	3	3	3
10	Does the curriculum train you on critical, logical problem-solving techniques?	3	3	3	3	3	3
11	Whether curriculum is providing basic knowledge of technologies related to other domains?	3	3	3	3	3	3
	Average						

Any suggestions:

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B. K

Signature

PO-ATTAINMENT															
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
INTERNAL	CO1	9	9	6	6	9	3	3	-	-	6	6	9	9	6
	CO2	9	6	6	9	9	6	6	-	-	6	6	9	9	6
	CO3	9	6	9	6	6	3	3	-	-	3	6	9	9	6
	CO4	9	9	9	9	9	3	6	-	-	6	6	9	9	6
	CO5	9	9	9	9	6	6	6	-	-	6	6	9	9	6
UNIVERSITY	CO1	3	3	2	2	3	1	1	-	-	2	2	3	3	2
	CO2	3	2	2	3	3	2	2	-	-	2	2	3	3	2
	CO3	3	2	3	2	2	1	1	-	-	1	2	3	3	2
	CO4	3	3	3	3	3	1	2	-	-	2	2	3	3	2
	CO5	3	3	3	3	2	2	2		-	2	2	3	3	2
OVERALL	CO1	2	2	2	2	2	2	2	2	2	2	2	2	2	2
	CO2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
	CO3	2	2	2	2	2	2	2	2	2	2	2	2	2	2
	CO4	2	2	2	2	2	2	2	2	2	2	2	2	2	2
	CO5	2	2	2	2	2	2	2	2	2	2	2	2	2	2
Attainment		2	2	2	2	2	2	2	2	2	2	2	2	2	2

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SIDDHARTHA INSTITUTE OF ENGINEERING & TECHNOLOGY			
DEPARTMENT			
PROGRAM OUTCOME ATTAINMENT			
Name of Faculty:	T KRISHNARJUNA RAO	Academic Year	2018-19
Branch & Section:	ECE	Exam:	PDC
Course:	B.TECH	Semester:	II

COURSE OUTCOME ATTAINMENT				
Course outcome attainment	Ist Mid	IInd Mid	Int	Univ
Course outcome - 1	3		3	2
Course outcome - 2	3		3	2
Course outcome - 3	3	3	3	2
Course outcome - 4		3	3	2
Course outcome - 5		3	3	2

COURSE OUTCOMES AND PROGRAM OUTCOMES MAPPING														
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2
Course outcome - 1	3	3	2	2	3	1	1	-	-	2	2	3	3	2
Course outcome - 2	3	2	2	3	3	2	2	-	-	2	2	3	3	2
Course outcome - 3	3	2	3	2	2	1	1	-	-	1	2	3	3	2
Course outcome - 4	3	3	3	3	3	1	2	-	-	2	2	3	3	2
Course outcome - 5	3	3	3	3	2	2	2		-	2	2	3	3	2
AVERAGE	3	2.6	2.6	2.6	2.6	1.4	1.6	-	-	1.8	2	3	3	2

SIDDHARTHA INSTITUTE OF ENGINEERING & TECHNOLOGY			
Department:			
Overall Course Outcome Attainment			
Name of the faculty :	T KRISHNARJUNA RAO	Academic Year:	2018-19
Branch & Section:	ECE	Exam:	PDC
Course:	B.TECH	Semester:	II

Course Outcomes	1st Internal Exam	2nd Internal Exam	Internal Exam	University Exam
Course outcome - 1	3		3	2
Course outcome - 2	3		3	2
Course outcome - 3	3	3	3	2
Course outcome - 4		3	3	2
Course outcome - 5		3	3	2

Course Outcomes		Attainment Level
Course outcome - 1	Ability to know the applications of diode as integrator, differentiator, clippers, and clamper circuits.	2
Course outcome - 2	To Learn various switching devices such as diode, transistor, SCR. Difference between logic gates and sampling gates	2
Course outcome - 3	To know the Differences between logic gates and sampling gates	2
Course outcome - 4	Design multivibrators for various applications, synchronization techniques and sweep circuits.	2
Course outcome - 5	Realizing logic gates using diodes and transistors	2
Average Attainment		2

Overall Course Attainment	2

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91	18TP5A0414	37
92	18TP5A0415	37
93	18TP5A0416	37
94	18TP5A0417	37
95	18TP5A0418	21
96	18TP5A0419	37
97	18TP5A0420	37
98	18TP5A0421	37
99	18TP5A0422	37
100	18TP5A0424	44
101	18TP5A0425	Ab
102	18TP5A0426	37
103	18TP5A0427	59
104	18TP5A0428	37
105	18TP5A0429	44
106	18TP5A0430	44
107	18TP5A0431	21
108	18TP5A0432	44
109	18TP5A0433	37
110	18TP5A0435	Ab
111	18TP5A0436	37
112	18TP5A0437	37
113	18TP5A0438	37
114	18TP5A0439	21
No. of students who scored more than the target score		89
No. of students who were successful in the subject		89
Percentage of students who scored more than target score		78.7
Attainment level		**2**

isnumber	level	final level
TRUE	2	2

63	17TP1A0466	44
64	17TP1A0467	44
65	17TP1A0469	44
66	17TP1A0472	21
67	17TP1A0473	37
68	17TP1A0474	21
69	17TP1A0475	37
70	17TP1A0476	21
71	17TP1A0477	44
72	17TP1A0479	37
73	17TP1A0480	44
74	17TP1A0481	37
75	17TP1A0482	44
76	17TP1A0483	37
77	17TP1A0484	44
78	17TP1A0485	44
79	17UR1A0401	44
80	17UR1A0404	59
81	18TP5A0402	37
82	18TP5A0404	37
83	18TP5A0405	21
84	18TP5A0407	Ab
85	18TP5A0408	44
86	18TP5A0409	44
87	18TP5A0410	21
88	18TP5A0411	Ab
89	18TP5A0412	Ab
90	18TP5A0413	37

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35	17TP1A0435	44
36	17TP1A0436	44
37	17TP1A0437	44
38	17TP1A0438	44
39	17TP1A0439	44
40	17TP1A0441	21
41	17TP1A0442	44
42	17TP1A0443	21
43	17TP1A0444	44
44	17TP1A0445	37
45	17TP1A0446	44
46	17TP1A0447	44
47	17TP1A0448	44
48	17TP1A0449	44
49	17TP1A0450	44
50	17TP1A0451	44
51	17TP1A0452	44
52	17TP1A0453	44
53	17TP1A0454	44
54	17TP1A0455	44
55	17TP1A0457	44
56	17TP1A0458	44
57	17TP1A0459	44
58	17TP1A0460	21
59	17TP1A0461	44
60	17TP1A0462	44
61	17TP1A0464	44
62	17TP1A0465	44

7	17TP1A0402	21
8	17TP1A0403	44
9	17TP1A0404	44
10	17TP1A0405	44
11	17TP1A0406	44
12	17TP1A0407	44
13	17TP1A0408	44
14	17TP1A0409	44
15	17TP1A0411	44
16	17TP1A0412	44
17	17TP1A0413	44
18	17TP1A0414	44
19	17TP1A0416	21
20	17TP1A0417	44
21	17TP1A0418	21
22	17TP1A0419	19
23	17TP1A0420	44
24	17TP1A0421	37
25	17TP1A0423	21
26	17TP1A0424	21
27	17TP1A0425	19
28	17TP1A0427	44
29	17TP1A0428	44
30	17TP1A0430	44
31	17TP1A0431	44
32	17TP1A0432	21
33	17TP1A0433	44
34	17TP1A0434	44

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Ranga Reddy District-501 506.

116.	18TP5A0439	1	1			0	1
Total Students more than target score Count		90	57	18	71	111	107
% students greater than target		100	98.2	100	100	94.8	92.2

Attainment Level	Overall attainment
1	>=60%
2	>=70%
3	>=80%

SIDDHARTHA INSTITUTE OF ENGINEERING & TECHNOLOGY			
Department:			
Overall Course Outcome Attainment as per University result			
Name of the faculty :	T KRISHNARJUNA RAO	Academic Year:	2018-2019
Branch & Section:	ECE- A	Exam:	PDC
Course:	B.TECH	Semester:	II

Sl.No	REG. NO	TOTAL Max score: 75
1	15TP1A04A1	15
2	16TP1A0410	24
3	16TP1A0428	44
4	16TP1A0434	21
5	16TP1A0447	19
6	17TP1A0401	44

88.	18TP5A0410	1	1			0	1
89.	18TP5A0411	1	0			1	1
90.	18TP5A0412	1	1			1	1
91.	18TP5A0413	1	1			1	1
92.	18TP5A0414	1			1	0	1
93.	18TP5A0415	1	1			1	1
94.	18TP5A0416	1		1		1	1
95.	18TP5A0417	1			1	1	1
96.	18TP5A0418	1	1			1	1
97.	18TP5A0419		1	1		1	1
98.	18TP5A0420	1	1			1	1
99.	18TP5A0421	1	1			1	1
100.	18TP5A0422	1	1			1	0
101.	18TP5A0423	1			1	1	1
102.	18TP5A0424	1	1			1	1
103.	18TP5A0425	1		1		1	1
104.	18TP5A0426	1	1			1	1
105.	18TP5A0427	1	1			1	1
106.	18TP5A0428		1	1		1	1
107.	18TP5A0429	1			1	1	1
108.	18TP5A0430	1			1	1	1
109.	18TP5A0431	1			1	1	1
110.	18TP5A0432	1	1			1	1
111.	18TP5A0433	1			1	1	1
112.	18TP5A0435	1			1	1	1
113.	18TP5A0436	1		1		0	1
114.	18TP5A0437	1	1			1	1
115.	18TP5A0438	1			1	0	1

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60.	17TP1A0462	1			1	1	1
61.	17TP1A0464	1			1	1	1
62.	17TP1A0465			1	1	1	1
63.	17TP1A0466	1			1	1	1
64.	17TP1A0467	1	1			1	1
65.	17TP1A0469	1			1	1	1
66.	17TP1A0472	1	1			1	1
67.	17TP1A0473	1			1	1	1
68.	17TP1A0474	1			1	1	1
69.	17TP1A0475			1	1	1	1
70.	17TP1A0476	1	1			1	1
71.	17TP1A0477	1			1	1	1
72.	17TP1A0479	1			1	1	1
73.	17TP1A0480	1			1	1	1
74.	17TP1A0481	1			1	1	1
75.	17TP1A0482	1			1	1	1
76.	17TP1A0483	1			1	1	1
77.	17TP1A0484	1	1			1	1
78.	17TP1A0485	1			1	1	1
79.	17UR1A0401	1			1	1	1
80.	17UR1A0404	1	1			1	1
81.	18TP5A0401	1			1	1	1
82.	18TP5A0402	1	1			1	1
83.	18TP5A0404	1	1			0	0
84.	18TP5A0405		1	1		0	1
85.	18TP5A0407	1	1			1	1
86.	18TP5A0408	1			1	1	1
87.	18TP5A0409	1			1	1	1

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32.	17TP1A0432	1	1			1	0
33.	17TP1A0433	1			1	1	1
34.	17TP1A0434	1	1			1	1
35.	17TP1A0435		1		1	1	1
36.	17TP1A0436	1			1	1	1
37.	17TP1A0437	1			1	1	1
38.	17TP1A0438	1			1	1	1
39.	17TP1A0439	1			1	1	1
40.	17TP1A0441		1		1	1	1
41.	17TP1A0442		1		1	1	1
42.	17TP1A0443		1		1	1	1
43.	17TP1A0444	1			1	1	1
44.	17TP1A0445	1			1	1	1
45.	17TP1A0446		1		1	1	1
46.	17TP1A0447		1		1	1	1
47.	17TP1A0448		1		1	1	1
48.	17TP1A0449			1	1	1	1
49.	17TP1A0450	1	1			1	1
50.	17TP1A0451	1		1		1	1
51.	17TP1A0452	1			1	1	1
52.	17TP1A0453		1		1	1	1
53.	17TP1A0454		1	1		1	1
54.	17TP1A0455	1			1	1	1
55.	17TP1A0457	1			1	1	1
56.	17TP1A0458	1	1			1	1
57.	17TP1A0459		1		1	1	1
58.	17TP1A0460	1			1	1	1
59.	17TP1A0461	1			1	1	1

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4.	16TP1A0434	1			1	1	0
5.	16TP1A0447	1	1			1	1
6.	17TP1A0401	1			1	1	1
7.	17TP1A0402			1	1	1	1
8.	17TP1A0403	1	1			1	1
9.	17TP1A0404	1	1			1	1
10.	17TP1A0405			1	1	1	1
11.	17TP1A0406		1		1	1	1
12.	17TP1A0407		1		1	1	1
13.	17TP1A0408	1			1	1	1
14.	17TP1A0409	1			1	1	1
15.	17TP1A0411			1	1	1	1
16.	17TP1A0412	1			1	1	1
17.	17TP1A0413	1			1	1	1
18.	17TP1A0414	1			1	1	1
19.	17TP1A0416		1		1	1	1
20.	17TP1A0417		1	1		1	0
21.	17TP1A0418		1	1		1	0
22.	17TP1A0419	1			1	1	0
23.	17TP1A0420	1			1	1	1
24.	17TP1A0421	1			1	1	1
25.	17TP1A0423	1	1			1	1
26.	17TP1A0424	1	1			1	1
27.	17TP1A0425	1			0	1	1
28.	17TP1A0427	1	1			1	1
29.	17TP1A0428	1			1	1	1
30.	17TP1A0430	1			1	1	1
31.	17TP1A0431				1	1	1

116.	18IP5A0439	4	4			3	4
Total Score		400	248	84	338	944	482
Total Number of students		90	58	18	71	117	116
Average Score		4.44	4.3	4.6	4.7	8	4
No. of students > target score		90	57	18	71	111	107
% of students > target score		100	98.2	100	100	94.8	92.2
Course Outcome Mapping with each Question							
Course outcome - 1							
Course outcome - 2							
Course outcome - 3						Y	
Course outcome - 4		Y	Y	Y		Y	
Course outcome - 5					Y	Y	
Course Outcome Attainment based on Exam Questions in terms of percentage of total students when mapped to each question							
Course outcome - 1							
Course outcome - 2							
Course outcome - 3						94.8	92.2
Course outcome - 4		100	98.2	100		94.8	92.2
Course outcome - 5					100	94.8	92.2
Attainment for all components		Subjective	Objective	Assignment	Overall	Attainment Level	
Course outcome - 1							
Course outcome - 2							
Course outcome - 3			94.8	92.2	94.5	3	
Course outcome - 4		99.33	94.8	92.2	95.44	3	
Course outcome - 5		100	94.8	92.2	95.6	3	
Overall Course attainment as average attainment level						3	

Sl.No	Roll Number	Target %= 50%					
		Question No.				Obj1	A1
Maximum Marks		1	2	3	4	10	5
Target score			2.5	2.5	2.5	5	2.5
1.	15TP1A04A1	1	1			1	0
2.	16TP1A0410	1	1			1	0
3.	16TP1A028		1			1	1

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Ranga Reddy District-501 506.

85.	18TP5A0407	4	4			5	5
86.	18TP5A0408	5			5	7	3
87.	18TP5A0409	5			5	7	3
88.	18TP5A0410	4	4			4	3
89.	18TP5A0411	4	2			5	5
90.	18TP5A0412	3	3			6	5
91.	18TP5A0413	4	5			6	5
92.	18TP5A0414	4			5	4	4
93.	18TP5A0415	3	4			5	5
94.	18TP5A0416	4		3		5	5
95.	18TP5A0417	5			5	5	5
96.	18TP5A0418	4	3			7	4
97.	18TP5A0419		5	5		5	4
98.	18TP5A0420	5	4			7	3
99.	18TP5A0421	4	4			7	3
100.	18TP5A0422	5	5			8	2
101.	18TP5A0423	5			3	5	3
102.	18TP5A0424	5	5			6	3
103.	18TP5A0425	4		4		7	4
104.	18TP5A0426	5	5			7	3
105.	18TP5A0427	5	5			7	4
106.	18TP5A0428		5	5		9	3
107.	18TP5A0429	5			5	9	3
108.	18TP5A0430	4			5	7	4
109.	18TP5A0431	4			5	5	5
110.	18TP5A0432	5	5			6	4
111.	18TP5A0433	5			5	7	4
112.	18TP5A0435	4			4	6	4
113.	18TP5A0436	4		4		4	3
114.	18TP5A0437	5	5			10	5
115.	18TP5A0438	4			4	4	3

54.	17TP1A0455	5			5	8	5
55.	17TP1A0457	4			3	9	4
56.	17TP1A0458	5	5			10	5
57.	17TP1A0459		5		5	10	5
58.	17TP1A0460	5			4	9	4
59.	17TP1A0461	5			5	10	5
60.	17TP1A0462	5			5	9	5
61.	17TP1A0464	4			5	9	4
62.	17TP1A0465			5	5	10	5
63.	17TP1A0466	4			5	9	4
64.	17TP1A0467	5	5			10	5
65.	17TP1A0469	4			5	10	5
66.	17TP1A0472	4	4			8	4
67.	17TP1A0473	4			4	8	4
68.	17TP1A0474	4			4	7	5
69.	17TP1A0475			5	5	10	5
70.	17TP1A0476	5	4			10	3
71.	17TP1A0477	4			5	10	3
72.	17TP1A0479	4			4	9	4
73.	17TP1A0480	4			5	10	3
74.	17TP1A0481	4			5	9	3
75.	17TP1A0482	5			5	9	5
76.	17TP1A0483	4			5	9	3
77.	17TP1A0484	5	3			10	5
78.	17TP1A0485	5			5	9	5
79.	17UR1A0401	5			5	10	5
80.	17UR1A0404	5	5			10	5
81.	18TP5A0401	3			3	5	4
82.	18TP5A0402	5	5			7	3
83.	18TP5A0404	4	5			4	2
84.	18TP5A0405		5	5		4	5

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Institute of Engineering & Technology,
Vinobha Nagar(V), Ibrahimpatnam(M),
Ranga Reddy District-501 506.

23.	17TP1A0420	5			5	10	5
24.	17TP1A0421	4			5	9	3
25.	17TP1A0423	5	5			9	3
26.	17TP1A0424	4	5			9	5
27.	17TP1A0425		4		2	6	5
28.	17TP1A0427	4	5			9	5
29.	17TP1A0428	5			5	10	5
30.	17TP1A0430	3			5	9	5
31.	17TP1A0431		5		5	8	5
32.	17TP1A0432	4	4			5	1
33.	17TP1A0433	5			5	8	5
34.	17TP1A0434	5	5			9	5
35.	17TP1A0435		3		4	9	3
36.	17TP1A0436	4			5	9	4
37.	17TP1A0437	4			5	9	5
38.	17TP1A0438	5			5	10	5
39.	17TP1A0439	5			5	10	5
40.	17TP1A0441		3		4	9	4
41.	17TP1A0442		5		5	10	5
42.	17TP1A0443		4		5	10	5
43.	17TP1A0444	5			5	10	5
44.	17TP1A0445	5			5	9	3
45.	17TP1A0446		5		5	10	5
46.	17TP1A0447		5		5	9	4
47.	17TP1A0448		5		5	10	5
48.	17TP1A0449			5	5	9	5
49.	17TP1A0450	5	5			10	5
50.	17TP1A0451	5		5		10	5
51.	17TP1A0452	5			5	10	5
52.	17TP1A0453		4		5	9	5
53.	17TP1A0454		5	5		10	5

SIDDHARTHA INSTITUTE OF ENGINEERING & TECHNOLOGY

Department:	EC E		
Course Outcome Attainment - Internal Assessments			
Name of the faculty :	T KRISHNARJUNA RAO	Academic Year:	2018-2019
Branch & Section:	ECE :A&B	Exam:	PDC INTERNAL-II
Course:	B.TECH	Semester :	II-SEM

S. No	Roll Number	Question No.				Objective	Assignment
		1	2	3	4		
Maximum Marks		5	5	5	5	10	5
1.	15TP1A04A1	4	4			6	2
2.	16TP1A0410	4	4			6	2
3.	16TP1A0428		5	5		8	5
4.	16TP1A0434	3			5	5	1
5.	16TP1A0447	4	3			5	3
6.	17TP1A0401	5			5	9	4
7.	17TP1A0402			5	5	9	5
8.	17TP1A0403	5	3			8	5
9.	17TP1A0404	5	4			10	5
10.	17TP1A0405			5	5	8	5
11.	17TP1A0406		5		5	10	5
12.	17TP1A0407		5		5	9	5
13.	17TP1A0408	4			5	9	5
14.	17TP1A0409	5			5	9	5
15.	17TP1A0411			5	5	8	5
16.	17TP1A0412	4			5	9	5
17.	17TP1A0413	5			5	9	5
18.	17TP1A0414	5			5	10	5
19.	17TP1A0416		3		5	8	4
20.	17TP1A0417		5	5		9	2
21.	17TP1A0418		3	3		6	2
22.	17TP1A0419	5			5	10	1

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PO-ATTAINMENT															
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
INTERNAL	CO1	9	9	6	6	9	3	3	-	-	6	6	9	9	6
	CO2	9	6	6	9	9	6	6	-	-	6	6	9	9	6
	CO3	9	6	9	6	6	3	3	-	-	3	6	9	9	6
	CO4	9	9	9	9	9	3	6	-	-	6	6	9	9	6
	CO5	9	9	9	9	6	6	6	-	-	6	6	9	9	6
UNIVERSITY	CO1	3	3	2	2	3	1	1	-	-	2	2	3	3	2
	CO2	3	2	2	3	3	2	2	-	-	2	2	3	3	2
	CO3	3	2	3	2	2	1	1	-	-	1	2	3	3	2
	CO4	3	3	3	3	3	1	2	-	-	2	2	3	3	2
	CO5	3	3	3	3	2	2	2		-	2	2	3	3	2
OVERALL	CO1	2	2	2	2	2	2	2	2	2	2	2	2	2	2
	CO2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
	CO3	2	2	2	2	2	2	2	2	2	2	2	2	2	2
	CO4	2	2	2	2	2	2	2	2	2	2	2	2	2	2
	CO5	2	2	2	2	2	2	2	2	2	2	2	2	2	2
Attainment		2	2	2	2	2	2	2	2	2	2	2	2	2	2

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COURSE OUTCOME ATTAINMENT				
Course outcome attainment	Ist Mid	IInd Mid	Int	Univ
Course outcome - 1	3		3	2
Course outcome - 2	3		3	2
Course outcome - 3	3	3	3	2
Course outcome - 4		3	3	2
Course outcome - 5		3	3	2

COURSE OUTCOMES AND PROGRAM OUTCOMES MAPPING														
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
Course outcome - 1	3	3	2	2	3	1	1	-	-	2	2	3	3	2
Course outcome - 2	3	2	2	3	3	2	2	-	-	2	2	3	3	2
Course outcome - 3	3	2	3	2	2	1	1	-	-	1	2	3	3	2
Course outcome - 4	3	3	3	3	3	1	2	-	-	2	2	3	3	2
Course outcome - 5	3	3	3	3	2	2	2		-	2	2	3	3	2
AVERAGE	3	2.6	2.6	2.6	2.6	1.4	1.6	-	-	1.8	2	3	3	2

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SIDDHARTHA INSTITUTE OF ENGINEERING & TECHNOLOGY			
Department:			
Overall Course Outcome Attainment			
Name of the faculty :	T KRISHNARJUNA RAO	Academic Year:	2018-19
Branch & Section:	ECE	Exam:	PDC
Course:	B.TECH	Semester:	II

Course Outcomes	1st Internal Exam	2nd Internal Exam	Internal Exam	University Exam
Course outcome - 1	3		3	2
Course outcome - 2	3		3	2
Course outcome - 3	3	3	3	2
Course outcome - 4		3	3	2
Course outcome - 5		3	3	2

Course Outcomes		Attainment Level
Course outcome - 1	Ability to know the applications of diode as integrator, differentiator, clippers, and clamper circuits.	2
Course outcome - 2	To Learn various switching devices such as diode, transistor, SCR. Difference between logic gates and sampling gates	2
Course outcome - 3	To know the Differences between logic gates and sampling gates	2
Course outcome - 4	Design multivibrators for various applications, synchronization techniques and sweep circuits.	2
Course outcome - 5	Realizing logic gates using diodes and transistors	2
Average Attainment		2

Overall Course Attainment	2

SIDDHARTHA INSTITUTE OF ENGINEERING & TECHNOLOGY			
DEPARTMENT			
PROGRAM OUTCOME ATTAINMENT			
Name of Faculty:	T KRISHNARJUNA RAO	Academic Year	2018-19
Branch & Section:	ECE	Exam:	PDC
Course:	B.TECH	Semester:	II

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104.	18TP5A0429	44
105.	18TP5A0430	44
106.	18TP5A0431	21
107.	18TP5A0432	44
108.	18TP5A0433	37
109.	18TP5A0435	Ab
110.	18TP5A0436	37
111.	18TP5A0437	37
112.	18TP5A0438	37
113.	18TP5A0439	21
No. of students who scored more than the target score		89
No. of students who were successful in the subject		89
Percentage of students who scored more than target score		78.7
Attainment level		**2**

isnumber	level	final level
TRUE	2	2

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79.	17UR1A0404	59
80.	18TP5A0402	37
81.	18TP5A0404	37
82.	18TP5A0405	21
83.	18TP5A0407	Ab
84.	18TP5A0408	44
85.	18TP5A0409	44
86.	18TP5A0410	21
87.	18TP5A0411	Ab
88.	18TP5A0412	Ab
89.	18TP5A0413	37
90.	18TP5A0414	37
91.	18TP5A0415	37
92.	18TP5A0416	37
93.	18TP5A0417	37
94.	18TP5A0418	21
95.	18TP5A0419	37
96.	18TP5A0420	37
97.	18TP5A0421	37
98.	18TP5A0422	37
99.	18TP5A0424	44
100.	18TP5A0425	Ab
101.	18TP5A0426	37
102.	18TP5A0427	59
103.	18TP5A0428	37

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54.	17TP1A0457	44
55.	17TP1A0458	44
56.	17TP1A0459	44
57.	17TP1A0460	21
58.	17TP1A0461	44
59.	17TP1A0462	44
60.	17TP1A0464	44
61.	17TP1A0465	44
62.	17TP1A0466	44
63.	17TP1A0467	44
64.	17TP1A0469	44
65.	17TP1A0472	21
66.	17TP1A0473	37
67.	17TP1A0474	21
68.	17TP1A0475	37
69.	17TP1A0476	21
70.	17TP1A0477	44
71.	17TP1A0479	37
72.	17TP1A0480	44
73.	17TP1A0481	37
74.	17TP1A0482	44
75.	17TP1A0483	37
76.	17TP1A0484	44
77.	17TP1A0485	44
78.	17UR1A0401	44

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29.	17TP1A0430	44
30.	17TP1A0431	44
31.	17TP1A0432	21
32.	17TP1A0433	44
33.	17TP1A0434	44
34.	17TP1A0435	44
35.	17TP1A0436	44
36.	17TP1A0437	44
37.	17TP1A0438	44
38.	17TP1A0439	44
39.	17TP1A0441	21
40.	17TP1A0442	44
41.	17TP1A0443	21
42.	17TP1A0444	44
43.	17TP1A0445	37
44.	17TP1A0446	44
45.	17TP1A0447	44
46.	17TP1A0448	44
47.	17TP1A0449	44
48.	17TP1A0450	44
49.	17TP1A0451	44
50.	17TP1A0452	44
51.	17TP1A0453	44
52.	17TP1A0454	44
53.	17TP1A0455	44

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5.	16TP1A0447	19
6.	17TP1A0401	44
7.	17TP1A0402	21
8.	17TP1A0403	44
9.	17TP1A0404	44
	17TP1A0405	44
10.	17TP1A0406	44
11.	17TP1A0407	44
12.	17TP1A0408	44
13.	17TP1A0409	44
14.	17TP1A0411	44
15.	17TP1A0412	44
16.	17TP1A0413	44
17.	17TP1A0414	44
18.	17TP1A0416	21
19.	17TP1A0417	44
20.	17TP1A0418	21
21.	17TP1A0419	19
22.	17TP1A0420	44
23.	17TP1A0421	37
24.	17TP1A0423	21
25.	17TP1A0424	21
26.	17TP1A0425	19
27.	17TP1A0427	44
28.	17TP1A0428	44

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120.	18TP5A0439	1	1			0	1
Total more than target score Count		90	57	18	71	111	107
% students greater than target		100	98.2	100	100	94.8	92.2

Attainment Level	Overall attainment
1	>=60%
2	>=70%
3	>=80%

SIDDHARTHA INSTITUTE OF ENGINEERING & TECHNOLOGY			
Department:			
Overall Course Outcome Attainment as per University result			
Name of the faculty :	T KRISHNARJUNA RAO	Academic Year:	2018-2019
Branch & Section:	ECE- A	Exam:	PDC
Course:	B.TECH	Semester:	II

Sl.No	REG. NO	TOTAL Max score: 75
1.	15TP1A04A1	15
2.	16TP1A0410	24
3.	16TP1A0428	44
4.	16TP1A0434	21

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94.	18TP5A0413	1	1			1	1
95.	18TP5A0414	1			1	0	1
96.	18TP5A0415	1	1			1	1
97.	18TP5A0416	1		1		1	1
98.	18TP5A0417	1			1	1	1
99.	18TP5A0418	1	1			1	1
100.	18TP5A0419		1	1		1	1
101.	18TP5A0420	1	1			1	1
102.	18TP5A0421	1	1			1	1
103.	18TP5A0422	1	1			1	0
104.	18TP5A0423	1			1	1	1
105.	18TP5A0424	1	1			1	1
106.	18TP5A0425	1		1		1	1
107.	18TP5A0426	1	1			1	1
108.	18TP5A0427	1	1			1	1
109.	18TP5A0428		1	1		1	1
110.	18TP5A0429	1			1	1	1
111.	18TP5A0430	1			1	1	1
112.	18TP5A0431	1			1	1	1
113.	18TP5A0432	1	1			1	1
114.	18TP5A0433	1			1	1	1
115.	18TP5A0434	1	1			1	
116.	18TP5A0435	1			1	1	1
117.	18TP5A0436	1		1		0	1
118.	18TP5A0437	1	1			1	1
119.	18TP5A0438	1				0	1

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68.	17TP1A0473	1			1	1	1
69.	17TP1A0474	1			1	1	1
70.	17TP1A0475			1	1	1	1
71.	17TP1A0476	1	1			1	1
72.	17TP1A0477	1			1	1	1
73.	17TP1A0479	1			1	1	1
74.	17TP1A0480	1			1	1	1
75.	17TP1A0481	1			1	1	1
76.	17TP1A0482	1			1	1	1
77.	17TP1A0483	1			1	1	1
78.	17TP1A0484	1	1			1	1
79.	17TP1A0485	1			1	1	1
80.	17UR1A0401	1			1	1	1
81.	17UR1A0404	1	1			1	1
82.	18TP5A0401	1			1	1	1
83.	18TP5A0402	1	1			1	1
84.	18TP5A0403						
85.	18TP5A0404	1	1			0	0
86.	18TP5A0405		1	1		0	1
87.	18TP5A0406					1	
88.	18TP5A0407	1	1			1	1
89.	18TP5A0408	1			1	1	1
90.	18TP5A0409	1			1	1	1
91.	18TP5A0410	1	1			0	1
92.	18TP5A0411	1	0			1	1
93.	18TP5A0412	1	1			1	1

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42.	17TP1A0442		1		1	1	1
43.	17TP1A0443		1		1	1	1
44.	17TP1A0444	1			1	1	1
45.	17TP1A0445	1			1	1	1
46.	17TP1A0446		1		1	1	1
47.	17TP1A0447		1		1	1	1
48.	17TP1A0448		1		1	1	1
49.	17TP1A0449			1	1	1	1
50.	17TP1A0450	1	1			1	1
51.	17TP1A0451	1		1		1	1
52.	17TP1A0452	1			1	1	1
53.	17TP1A0453		1		1	1	1
54.	17TP1A0454		1	1		1	1
55.	17TP1A0455	1			1	1	1
56.	17TP1A0457	1			1	1	1
57.	17TP1A0458	1	1			1	1
58.	17TP1A0459		1		1	1	1
59.	17TP1A0460	1			1	1	1
60.	17TP1A0461	1			1	1	1
61.	17TP1A0462	1			1	1	1
62.	17TP1A0464	1			1	1	1
63.	17TP1A0465			1	1	1	1
64.	17TP1A0466	1			1	1	1
65.	17TP1A0467	1	1			1	1
66.	17TP1A0469	1			1	1	1
67.	17TP1A0472	1	1			1	1

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Ranga Reddy District-501 506.

16.	17TP1A0412	1			1	1	1
17.	17TP1A0413	1			1	1	1
18.	17TP1A0414	1			1	1	1
19.	17TP1A0416		1		1	1	1
20.	17TP1A0417		1	1		1	0
21.	17TP1A0418		1	1		1	0
22.	17TP1A0419	1			1	1	0
23.	17TP1A0420	1			1	1	1
24.	17TP1A0421	1			1	1	1
25.	17TP1A0423	1	1			1	1
26.	17TP1A0424	1	1			1	1
27.	17TP1A0425	1			0	1	1
28.	17TP1A0426						
29.	17TP1A0427	1	1			1	1
30.	17TP1A0428	1			1	1	1
31.	17TP1A0430	1			1	1	1
32.	17TP1A0431		1		1	1	1
33.	17TP1A0432	1	1			1	0
34.	17TP1A0433	1			1	1	1
35.	17TP1A0434	1	1			1	1
36.	17TP1A0435		1		1	1	1
37.	17TP1A0436	1			1	1	1
38.	17TP1A0437	1			1	1	1
39.	17TP1A0438	1			1	1	1
40.	17TP1A0439	1			1	1	1
41.	17TP1A0441		1		1	1	1

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Ranga Reddy Dist. - 501 512.

Attainment for all components	Subjective	Objective	Assignment	Overall	Attainment Level
Course outcome - 1					
Course outcome - 2					
Course outcome - 3		94.8	92.2	94.5	3
Course outcome - 4	99.33	94.8	92.2	95.44	3
Course outcome - 5	100	94.8	92.2	95.6	3
Overall Course attainment as average attainment level					3

Sl.No	Roll Number	Target %= 50%					
		Question No.				Obj1	A1
Maximum Marks		1	2	3	4	5	5
			Target score	2.5	2.5	2.5	2.5
1.	15TP1A04A1	1	1			1	0
2.	16TP1A0410	1	1			1	0
3.	16TP1A028		1	1		1	1
4.	16TP1A0434	1			1	1	0
5.	16TP1A0447	1	1			1	1
6.	17TP1A0401	1			1	1	1
7.	17TP1A0402			1	1	1	1
8.	17TP1A0403	1	1			1	1
9.	17TP1A0404	1	1			1	1
10.	17TP1A0405			1	1	1	1
11.	17TP1A0406		1		1	1	1
12.	17TP1A0407		1		1	1	1
13.	17TP1A0408	1			1	1	1
14.	17TP1A0409	1			1	1	1
15.	17TP1A0411			1	1	1	1

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108.	18TP5A0427	5	5			7	4
109.	18TP5A0428		5	5		9	3
110.	18TP5A0429	5			5	9	3
111.	18TP5A0430	4			5	7	4
112.	18TP5A0431	4			5	5	5
113.	18TP5A0432	5	5			6	4
114.	18TP5A0433	5			5	7	4
115.	18TP5A0434	4	4			8	
116.	18TP5A0435	4			4	6	4
117.	18TP5A0436	4		4		4	3
118.	18TP5A0437	5	5			10	5
119.	18TP5A0438	4			4	4	3
120.	18TP5A0439	4	4			3	4
Total Score		400	248	84	338	944	482
Total Number of students		90	58	18	71	117	116
Average Score		4.44	4.3	4.6	4.7	8	4

No. of students > target score	90	57	18	71	111	107
% of students > target score	100	98.2	100	100	94.8	92.2

Course Outcome Mapping with each Question						
Course outcome - 1						
Course outcome - 2						
Course outcome - 3					Y	
Course outcome - 4	Y	Y	Y		Y	
Course outcome - 5				Y	Y	
Course Outcome Attainment based on Exam Questions in terms of percentage of total students when mapped to each question						
Course outcome - 1						
Course outcome - 2						
Course outcome - 3					94.8	92.2
Course outcome - 4	100	98.2	100		94.8	92.2
Course outcome - 5				100	94.8	92.2

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79.	17TP1A0485	5			5	9	5
80.	17UR1A0401	5			5	10	5
81.	17UR1A0404	5	5			10	5
82.	18TP5A0401	3			3	5	4
83.	18TP5A0402	5	5			7	3
84.	18TP5A0403						
85.	18TP5A0404	4	5			4	2
86.	18TP5A0405		5	5		4	5
87.	18TP5A0406						
88.	18TP5A0407	4	4			5	5
89.	18TP5A0408	5			5	7	3
90.	18TP5A0409	5			5	7	3
91.	18TP5A0410	4	4			4	3
92.	18TP5A0411	4	2			5	5
93.	18TP5A0412	3	3			6	5
94.	18TP5A0413	4	5			6	5
95.	18TP5A0414	4			5	4	4
96.	18TP5A0415	3	4			5	5
97.	18TP5A0416	4		3		5	5
98.	18TP5A0417	5			5	5	5
99.	18TP5A0418	4	3			7	4
100.	18TP5A0419		5	5		5	4
101.	18TP5A0420	5	4			7	3
102.	18TP5A0421	4	4			7	3
103.	18TP5A0422	5	5			8	2
104.	18TP5A0423	5			3	5	3
105.	18TP5A0424	5	5			6	3
106.	18TP5A0425	4		4		7	4
107.	18TP5A0426	5	5			7	3

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50.	17TP1A0450	5	5			10	5
51.	17TP1A0451	5		5		10	5
52.	17TP1A0452	5			5	10	5
53.	17TP1A0453		4		5	9	5
54.	17TP1A0454		5	5		10	5
55.	17TP1A0455	5			5	8	5
56.	17TP1A0457	4			3	9	4
57.	17TP1A0458	5	5			10	5
58.	17TP1A0459		5		5	10	5
59.	17TP1A0460	5			4	9	4
60.	17TP1A0461	5			5	10	5
61.	17TP1A0462	5			5	9	5
62.	17TP1A0464	4			5	9	4
63.	17TP1A0465			5	5	10	5
64.	17TP1A0466	4			5	9	4
65.	17TP1A0467	5	5			10	5
66.	17TP1A0469	4			5	10	5
67.	17TP1A0472	4	4			8	4
68.	17TP1A0473	4			4	8	4
69.	17TP1A0474	4			4	7	5
70.	17TP1A0475			5	5	10	5
71.	17TP1A0476	5	4			10	3
72.	17TP1A0477	4			5	10	3
73.	17TP1A0479	4			4	9	4
74.	17TP1A0480	4			5	10	3
75.	17TP1A0481	4			5	9	3
76.	17TP1A0482	5			5	9	5
77.	17TP1A0483	4			5	9	3
78.	17TP1A0484	5	3			10	5

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21.	17TP1A0418		3	3		6	2
22.	17TP1A0419	5			5	10	1
23.	17TP1A0420	5			5	10	5
24.	17TP1A0421	4			5	9	3
25.	17TP1A0423	5	5			9	3
26.	17TP1A0424	4	5			9	5
27.	17TP1A0425		4		2	6	5
28.	17TP1A0426						
29.	17TP1A0427	4	5			9	5
30.	17TP1A0428	5			5	10	5
31.	17TP1A0430	3			5	9	5
32.	17TP1A0431		5		5	8	5
33.	17TP1A0432	4	4			5	1
34.	17TP1A0433	5			5	8	5
35.	17TP1A0434	5	5			9	5
36.	17TP1A0435		3		4	9	3
37.	17TP1A0436	4			5	9	4
38.	17TP1A0437	4			5	9	5
39.	17TP1A0438	5			5	10	5
40.	17TP1A0439	5			5	10	5
41.	17TP1A0441		3		4	9	4
42.	17TP1A0442		5		5	10	5
43.	17TP1A0443		4		5	10	5
44.	17TP1A0444	5			5	10	5
45.	17TP1A0445	5			5	9	3
46.	17TP1A0446		5		5	10	5
47.	17TP1A0447		5		5	9	4
48.	17TP1A0448		5		5	10	5
49.	17TP1A0449			5	5	9	5

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CMOS compared to TTL:

- CMOS circuits do not draw as much power as TTL circuits while at rest. However, CMOS power consumption increases faster with higher clock speeds than TTL does. Lower current draw requires less power supply distribution, therefore causing a simpler and cheaper design.
- Due to longer rise and fall times, the transmission of digital signals becomes simpler and less expensive with CMOS chips.
- CMOS components are more susceptible to damage from electrostatic discharge than TTL components.

CMOS (complementary metal-oxide-semiconductor) technology is used predominantly to create digital circuitry. The fundamental building blocks of CMOS circuits are P-type and N-type MOSFET transistors. A P-type MOSFET can be modeled as a switch that is closed when the input voltage is low (0 V) and open when the input voltage is high (5 V). A N-type MOSFET can be modeled as a switch that is closed when the input voltage is high (5 V) and open when the input voltage is low (0 V). The basic idea for CMOS technology is to combine P-type and N-type MOSFETs such that there is never a conducting path from the supply voltage (5 V) to ground. As a consequence, CMOS circuits consume very little energy. CMOS technology employs two types of transistor: n-channel and p-channel. The two differ in the characteristics of the semiconductor materials used in their implementation and in the mechanism governing the conduction of a current through them. We will model this behavior using switches controlled by voltages corresponding to logic 0 and logic 1. Such a model ignores complex electronic devices and captures only logical behavior.

The symbol for an n-channel transistor is shown in Figure below . The transistor has three terminals: the gate (G), the source (S), and the drain (D). The voltage applied between G and S determines whether a path for current to flow exists between D and S. If a path exists, we say that the transistor is ON, and if a path does not exist, we say that the transistor is OFF. The n-channel transistor is ON if the applied gate-to-source voltage is H and OFF if the applied voltage is L. Here we will make the usual assumption that a 1 represents the H voltage range and a 0 represents the L voltage range. The notion of whether a path for current to flow exists is easily modeled by a switch. The switch consists of two fixed terminals corresponding to the S and D

terminals of the transistor. In addition, there is a movable contact that, depending on its position, determines whether the switch is open or closed. The position of the contact is controlled by the voltage applied to the gate terminal G. Since we are looking at logic behavior, this control voltage is represented on the symbol by the input variable X on the gate terminal. For an n-channel transistor, the contact is open (no path exists) for the input variable X equal to 0 and closed (a path exists) for the input variable X equal to 1. Such a contact is traditionally referred to as being normally open, that is, open without a positive voltage applied to activate or close it.

BiCmos Advantages and Disadvantages:

This page covers **BiCMOS** basics,advantages and disadvantages. It describes BiCMOS devices viz. BiCMOS Inverters, BiCMOS Gates and BiCMOS Drivers.

BiCMOS refers to logic family which combines both bipolar and CMOS logic devices in one single IC. Hence it offers following benefits:

- High Speed of operation
- High packing density
- Low Power Dissipation

As it is combination of bipolar and CMOS technologies it offers following benefits over conventional CMOS and Bipolar logic families. This is the main difference between them.

BiCMOS Advantages

Following are the advantages of BiCMOS:

- Low power dissipation compare to Bipolar
- Improved speed of operation compare to CMOS
- Large current drive compare to CMOS

BiCMOS Disadvantages

Following are the disadvantages of BiCMOS:

- High Cost

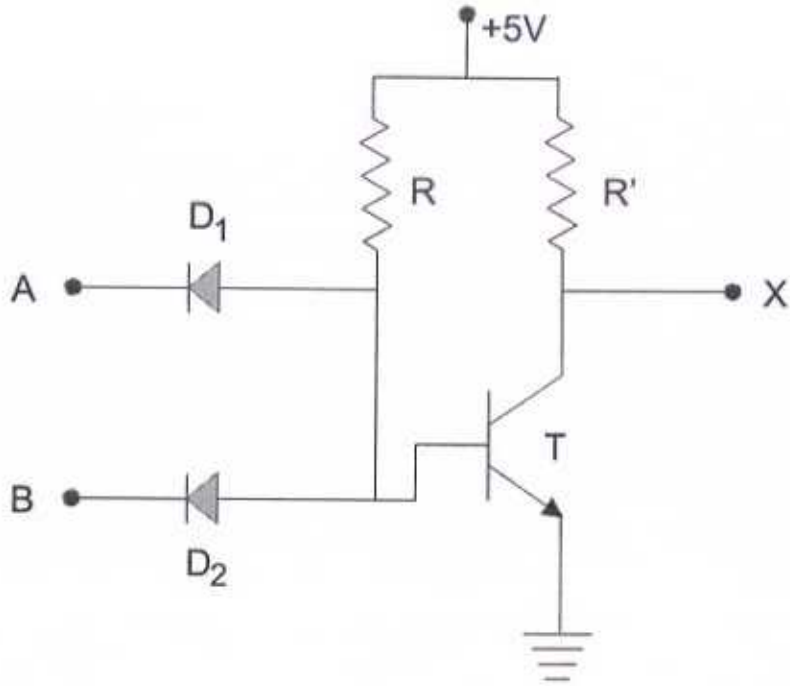
Diode and Transistor NAND Gate or DTL NAND Gate:

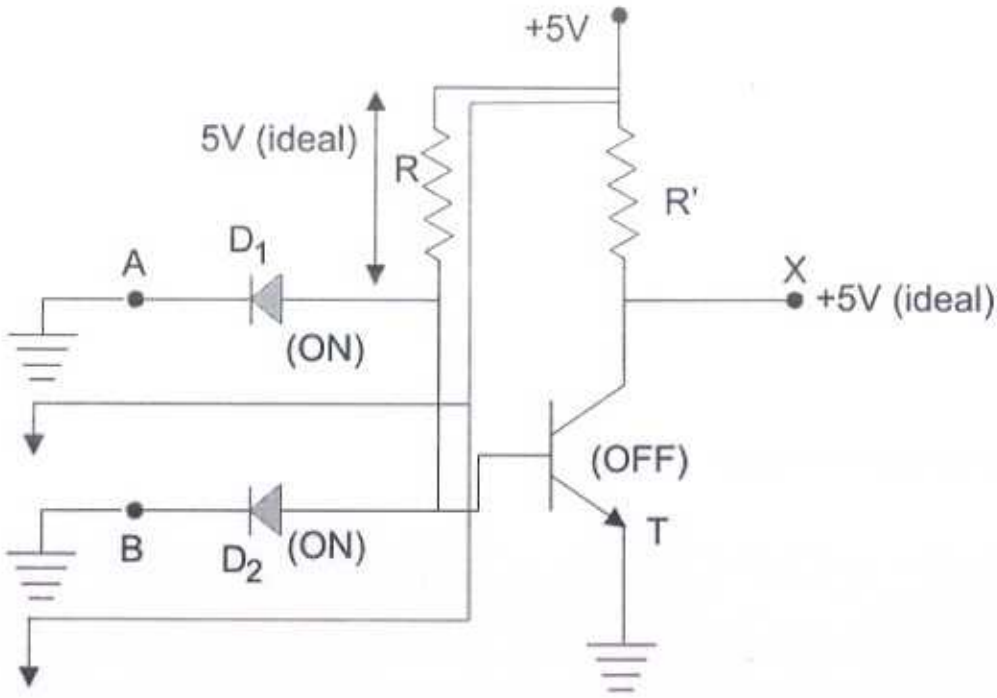
July 25, 2018 by Electrical4U

Realizing NAND Gate using Diode and Transistor

For simplicity we will show here only two inputs NAND gate circuit by using diodes and transistors. This NAND gate is called **DTL NAND gate** or **Diode Transistor Logical NAND Gate.**

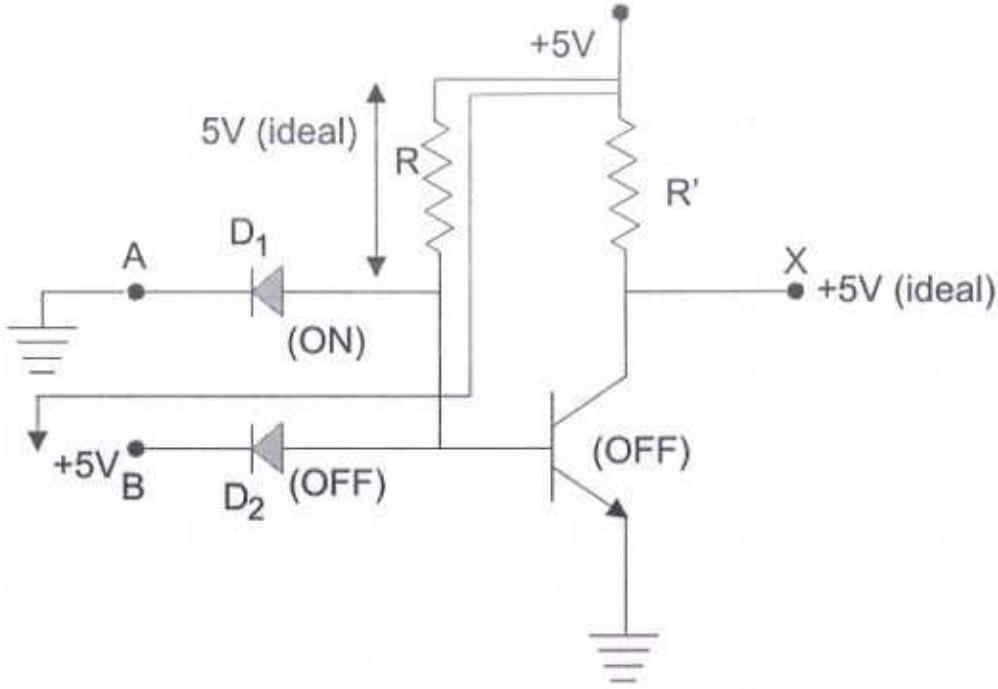
When both input A and B are given with 0 V, both of the diodes are in forward biased condition that is in ON condition. Supply voltage will get path to the ground through diode D_1 and D_2. Entire supply voltage +5 V will ideally drop across resistor R and hence base terminal of transistor T will not get enough potential to turn ON the transistor and hence the transistor will be in OFF condition. As a result supply voltage +5 V will appear at output terminal X and hence output X will become high or logical 1.

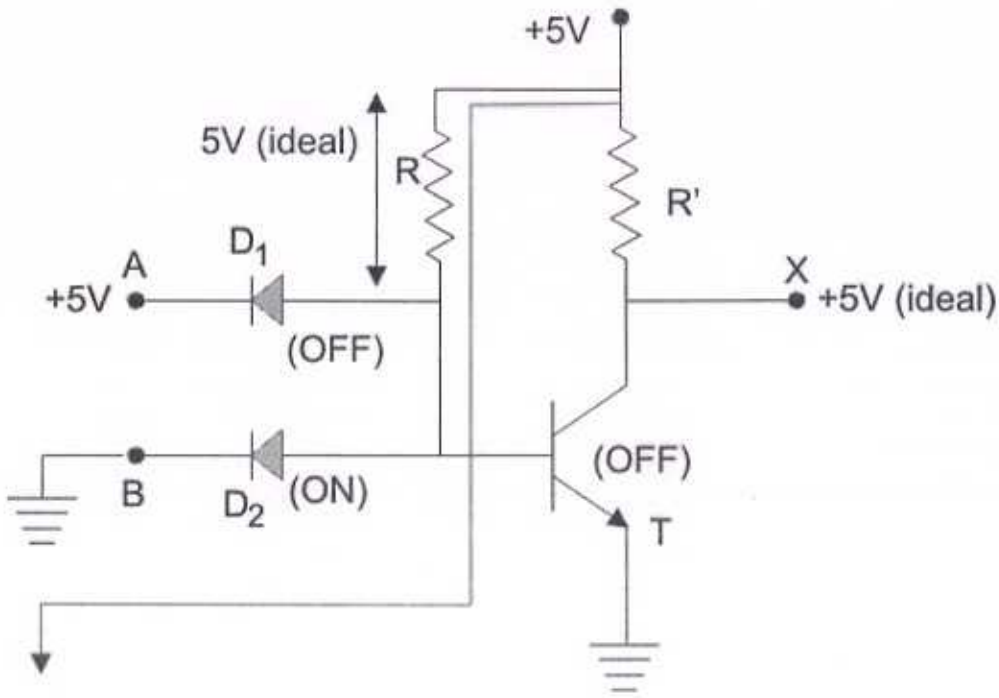




Now if either of diode D_1 and D_2, is applied with 0 V, the same thing happens as in these cases also the supply voltage gets a path to the ground either of the forward biased diode. In that cases

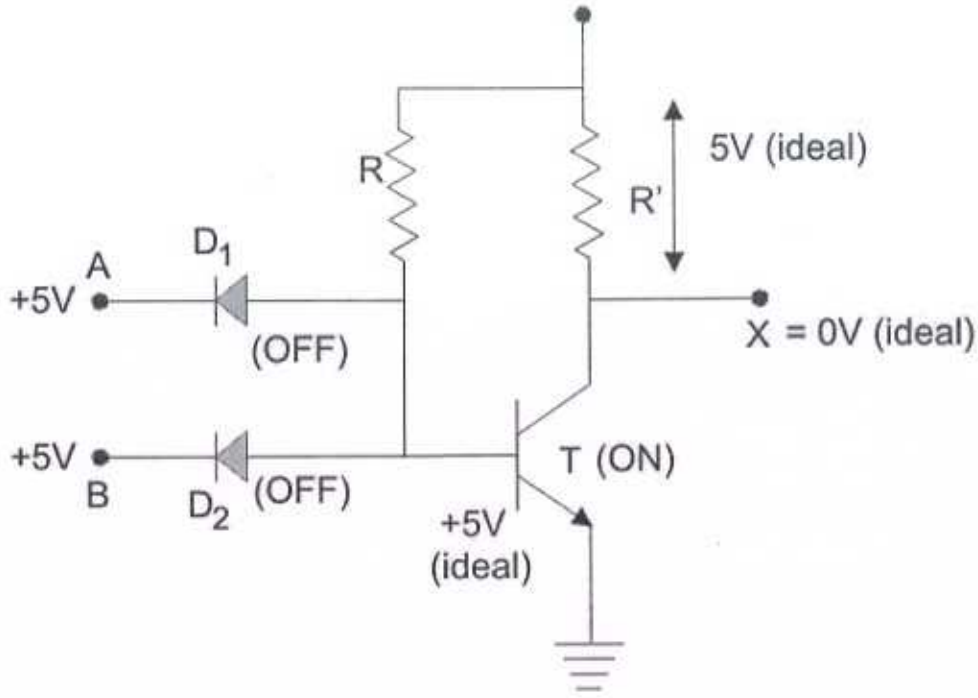
also the output will be logical high or 1.

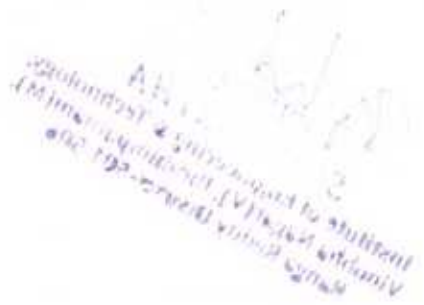


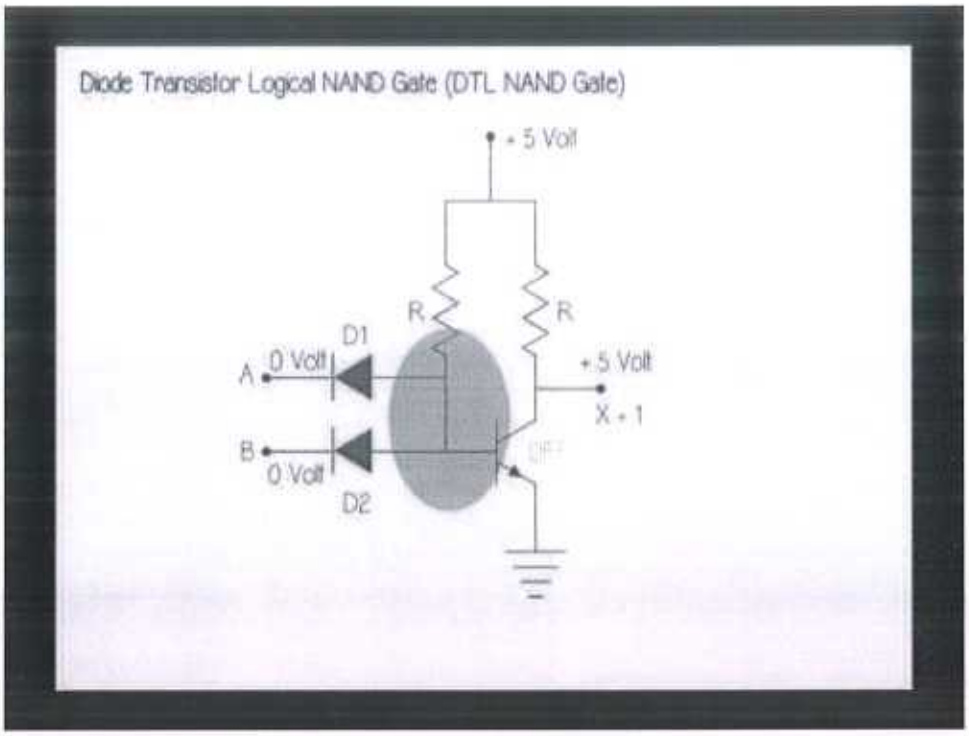


When both of the inputs are given with +5 V that is logical 1, both of the diodes are in OFF

condition and hence supply voltage will appear at the base terminal of the transistor T which makes it switched ON and supply voltage gets a path to the ground through this transistors. Ideally entire supply voltage +5 V will drop across resistor R' and output terminal X will get ideally zero volts and hence the output is considered as logical 0. Hence, the output is only 0 when and only when both inputs are +5 V or logical 1.







A two-input **NAND gate** produces a LOW output if both of its inputs are HIGH. It's easy enough to create a **NAND gate** by**using** just two **transistors**. A **NAND gate** circuit is almost identical to an AND **gate** circuit.

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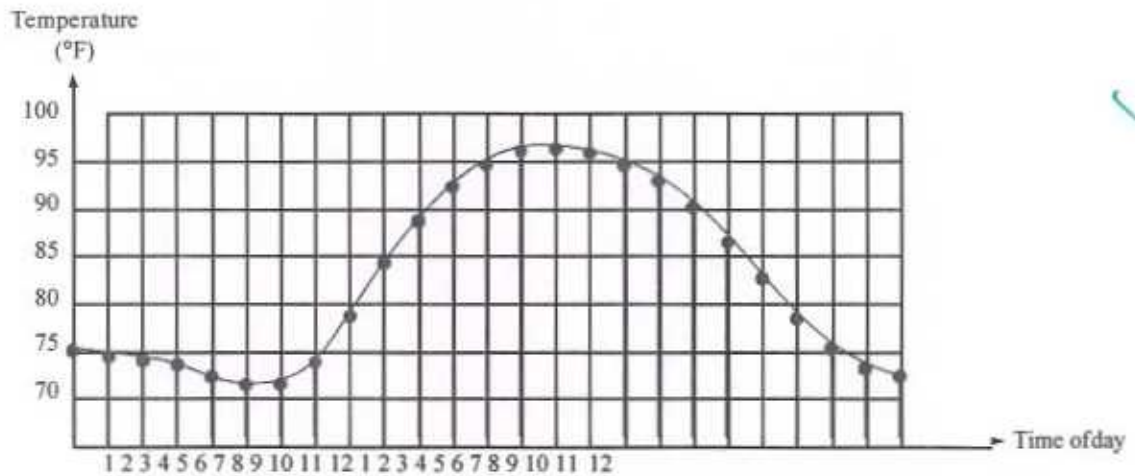
Basics

Analog Quantities

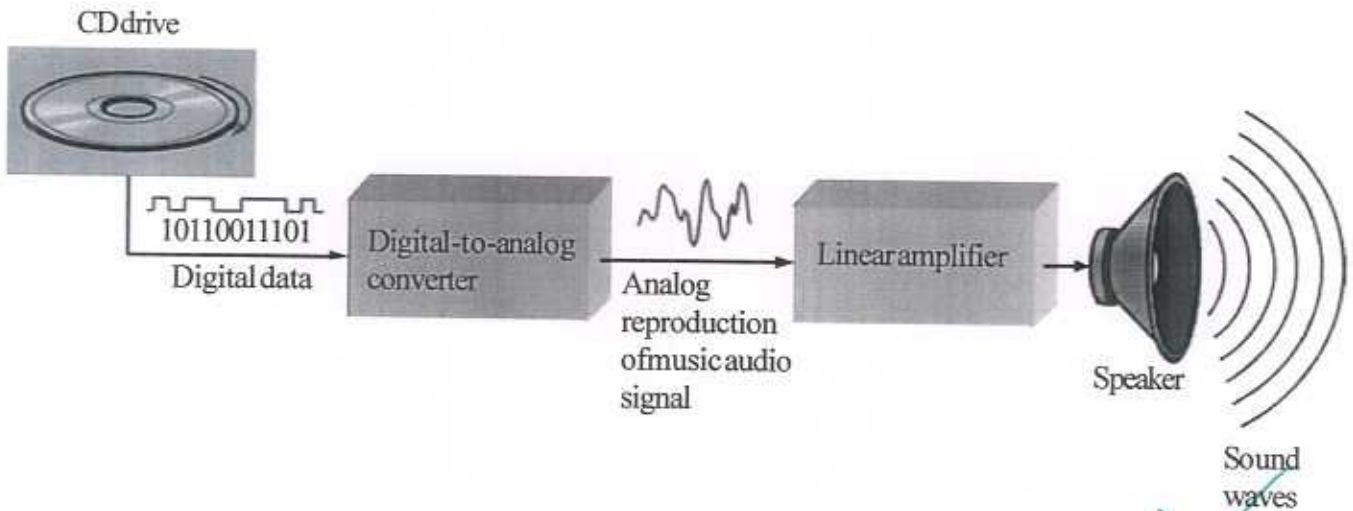
- Most natural quantities that we see are **analog** and vary continuously. Analog systems can generally handle higher power than digital systems



- Digital systems can process, store, and transmit data more efficiently but can only assign discrete values to each point

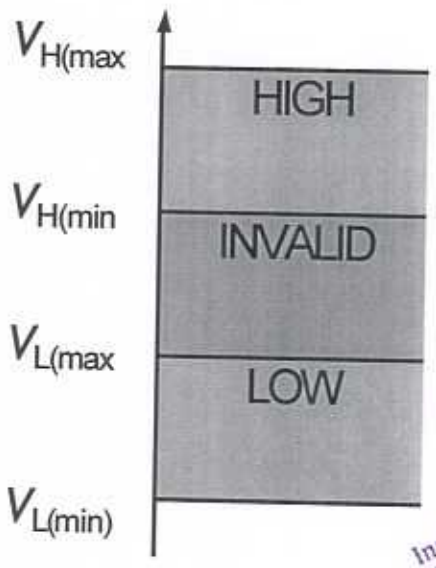
Analog and Digital Systems

- Digital systems can process, store, and transmit data more efficiently but can only assign discrete values to each point



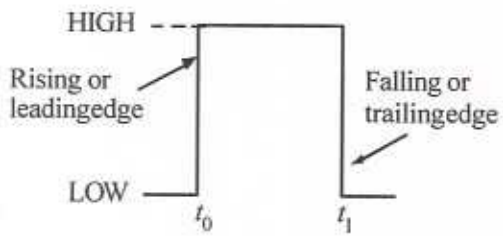
Contd..

- Digital electronics uses circuits that have two states, which are represented by two different voltage levels called HIGH and LOW. The voltages represent numbers in the binary system
- In binary, a single number is called a *bit* (for *b*inary dig*it*). A bit can have the value of either a 0 or a 1, depending on if the voltage is HIGH or LOW.

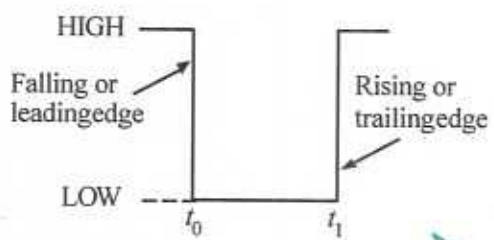


Digital Signals

- Digital waveforms change between the LOW and HIGH levels. A positive going pulse is one that goes from anormally LOW logic level to a HIGH level and then back again. Digital waveforms are made up of a series of pulses



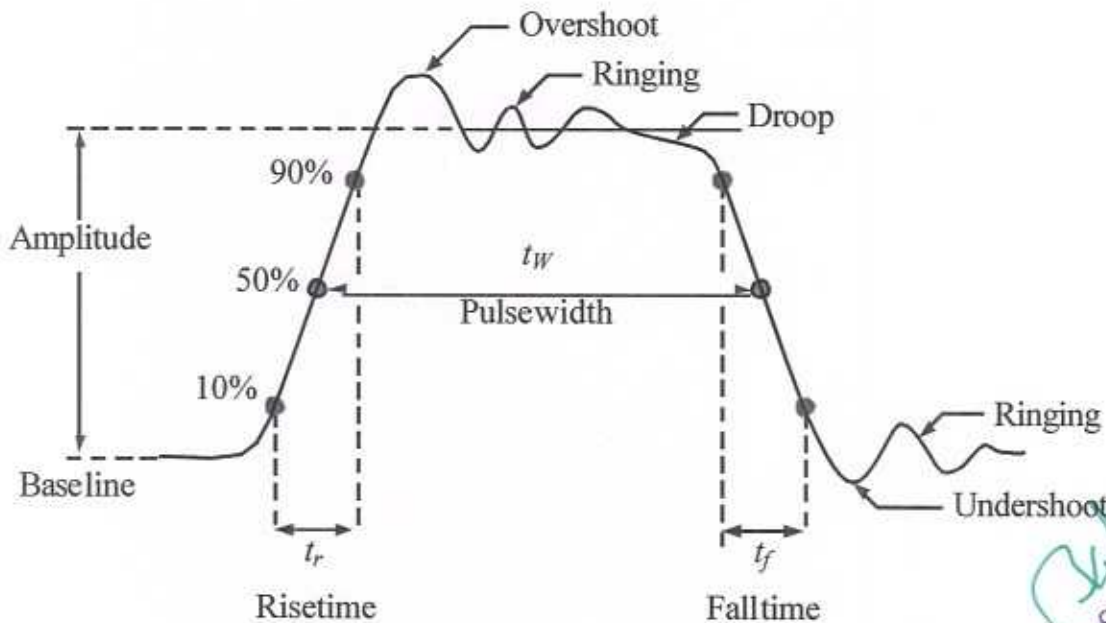
(a) Positive–goingpulse



(b)Negative–going pulse

Pulse Definitions

- Actual pulses are not ideal but are described by the rise time, fall time, amplitude, and other characteristics.



Periodic Pulse Waveforms

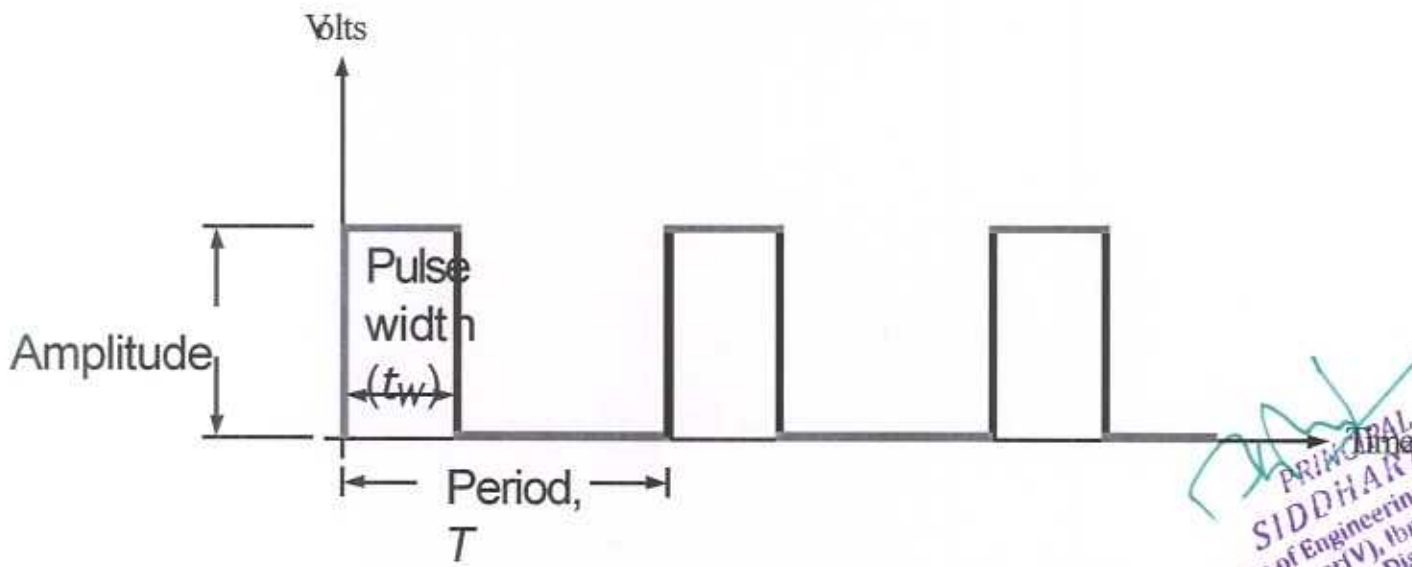
- Periodic pulse waveforms are composed of pulses that repeats in a fixed interval called the **period**.
- The **frequency** is the rate it repeats and is measured in hertz. The **clock** is a basic timing signal that is an example of a periodic wave.
-

$$T = \frac{1}{f} z$$

What is the period of a repetitive wave if $f = 3.2$ GHz?

Pulse Definitions

- In addition to frequency and period, repetitive pulse waveforms are described by the amplitude (A), pulse width (t_W) and duty cycle. Duty cycle is the ratio of t_W to T.



Advantages of Integrator over differentiator

- Integrators are almost invariably preferred over differentiators in analog computer applications for the following reasons.

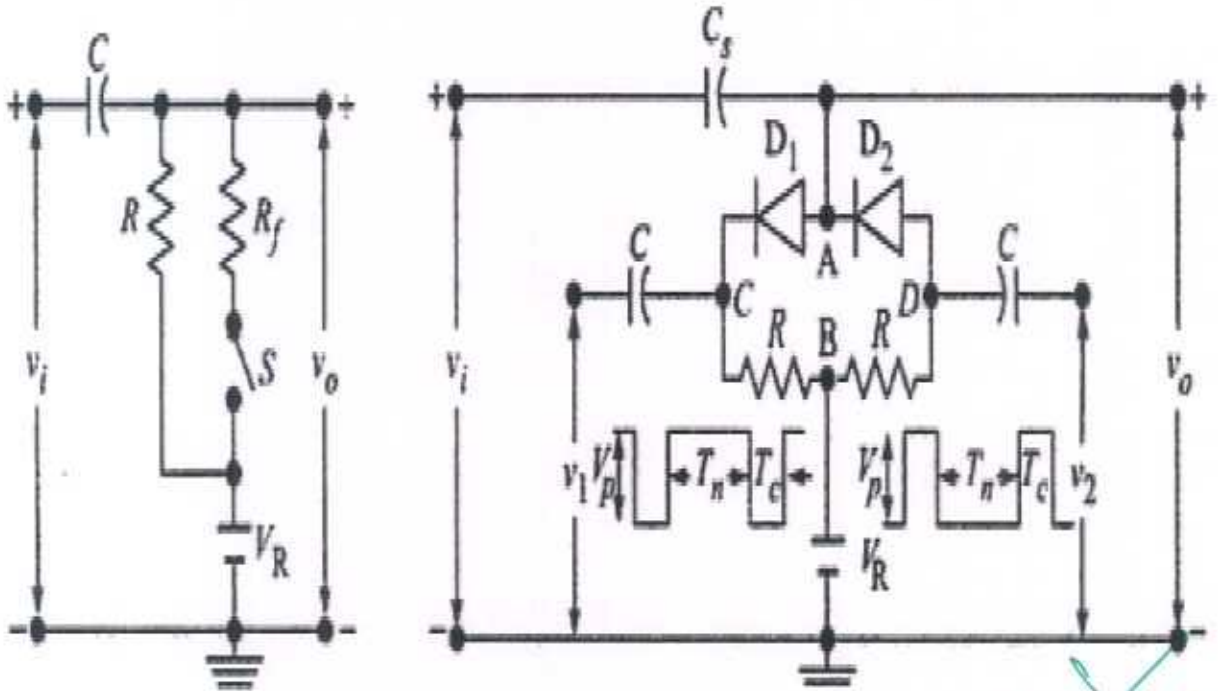
- The gain of the integrator decreases with frequency where as the gain of the differentiator increases linearly with frequency. It is easier to stabilize the former than the latter with respect to spurious oscillations.

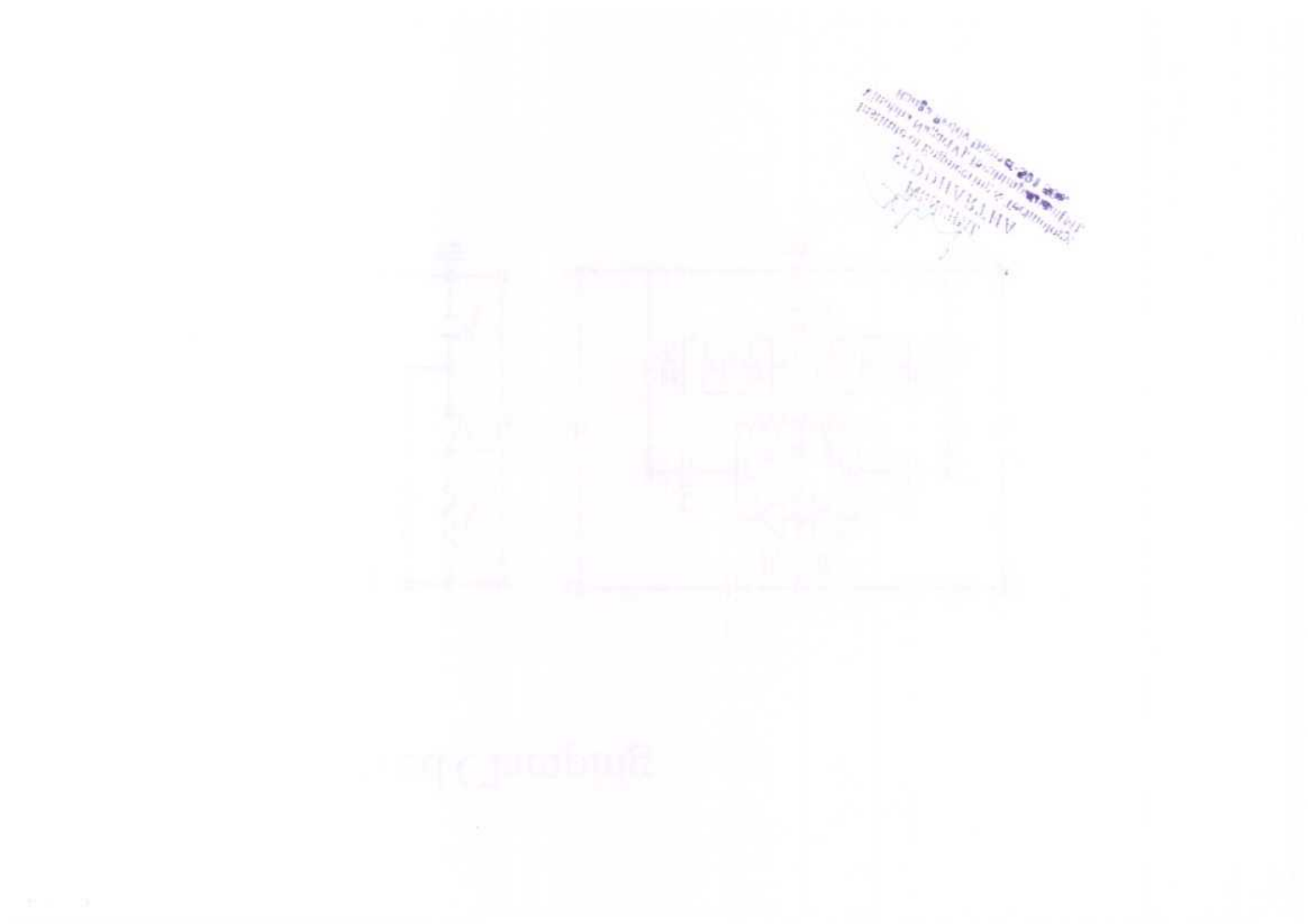
- As a result of its limited band width an integrator is less sensitive to noise voltages than a differentiator.

- If the input wave form changes very rapidly, the amplifier of a differentiator may over load.

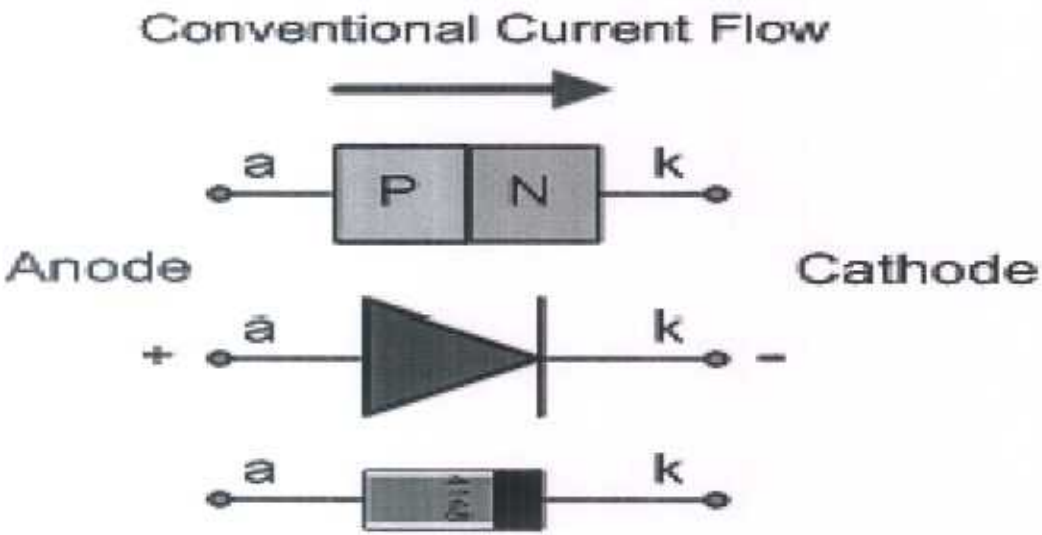
- It is more convenient to introduce initial conditions in an integrator.

Synchronized Clamping





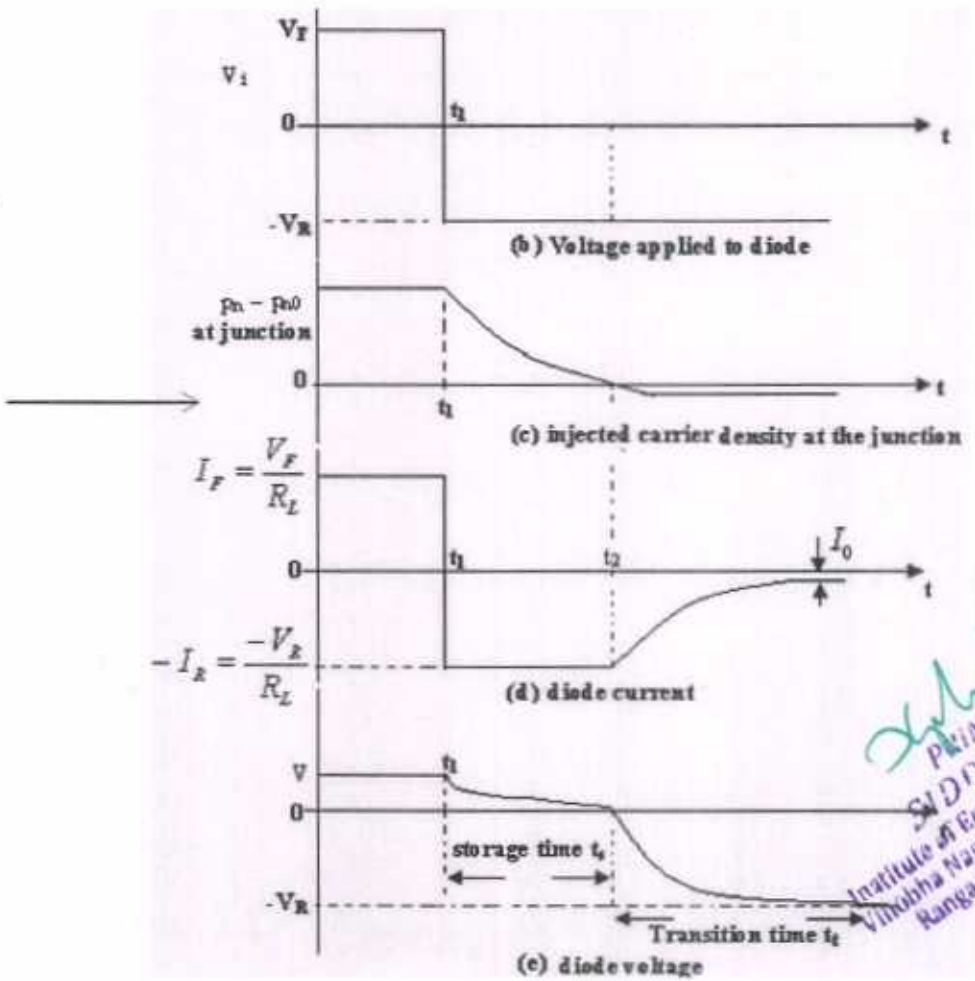
Diode As a Switch



Silicon Diode and its
V-I Characteristics

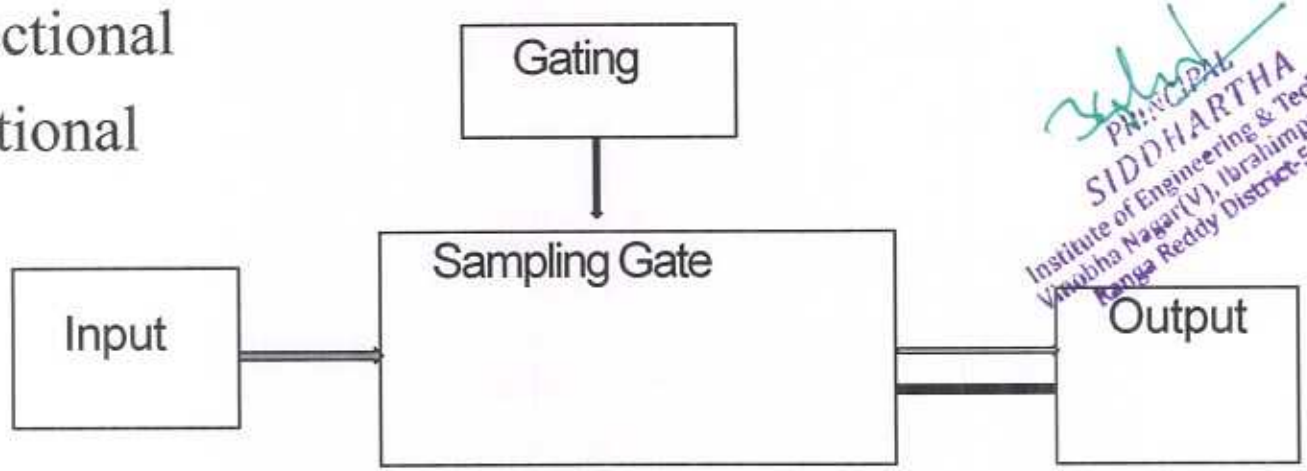
Diode Switching times

- Reverse recovery time of the diode
- Forward recovery time of the diode

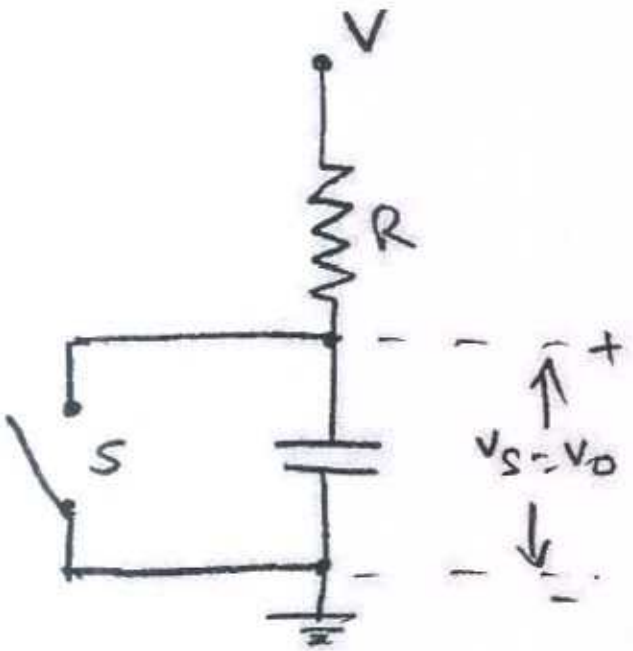


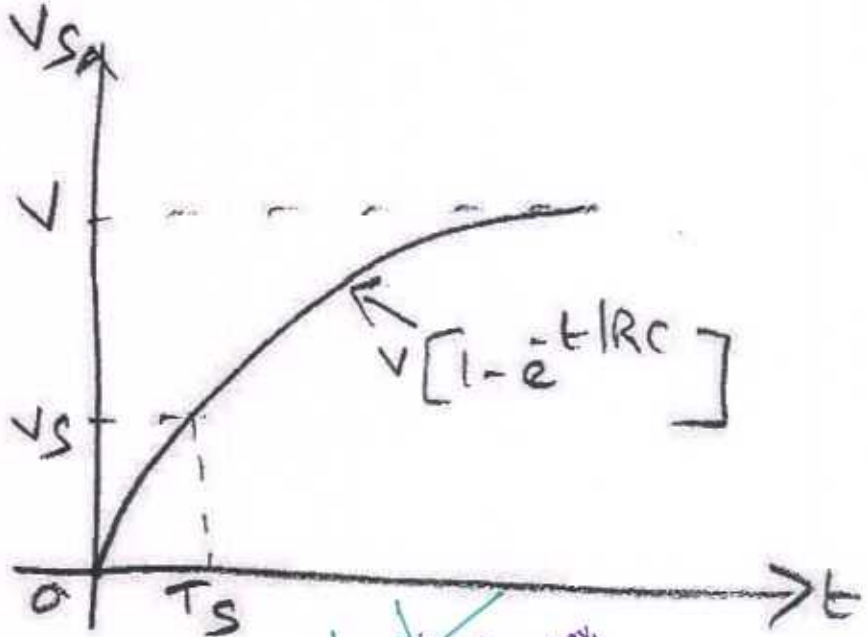
Sampling Gates

- Sampling Gates are also called as Transmission gates ,linear gates and selection circuits,in which the output is exact reproduction of the input during a selected time interval and zero otherwise.
- It has two inputs – gating signal, rectangular wave
- Two types
- Unidirectional
- Bidirectional



Exponential sweep circuit



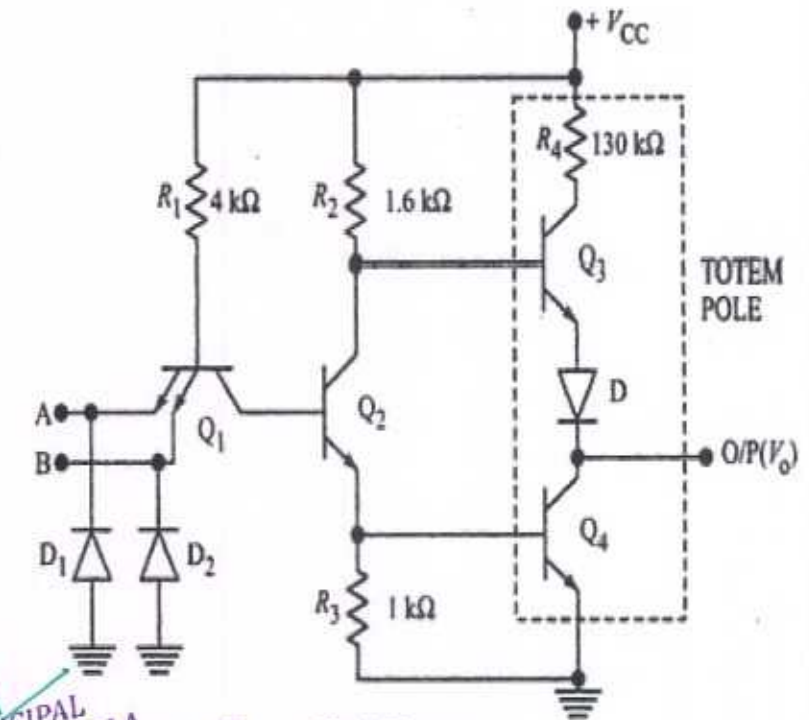


Comparision of Miller and Bootstrap time base generator

Bootstrap sweep circuit	Miller sweep circuit
1) The circuit employs positive feedback.	1) The circuit employs negative feedback.
2) The circuit generates positive going ramp.	2) The circuit generates negative going ramp.
3) The circuit employs an emitter follower whose gain is nearly unity.	3) The circuit requires an amplifier whose gain is very very large (ideally infinite).
4) The amplifier must have high input resistance.	4) Amplifier with high input resistance is not very essential.

TOTEM POLE NAND GATE

- First introduced by in 1964 (Texas Instruments)
- TTL has shaped digital technology in many ways
- Standard TTL family (e.g. 7400) is obsolete
- Newer TTL families still used (e.g. 74ALS00)

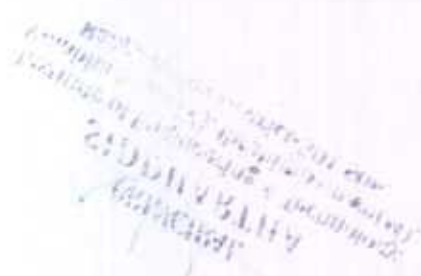


Circuit diagram

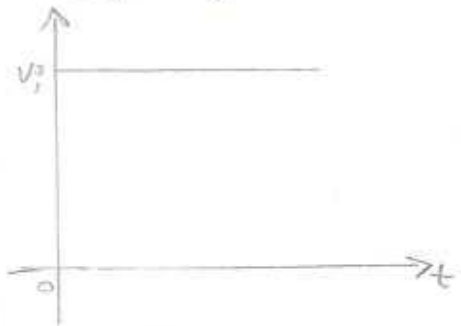
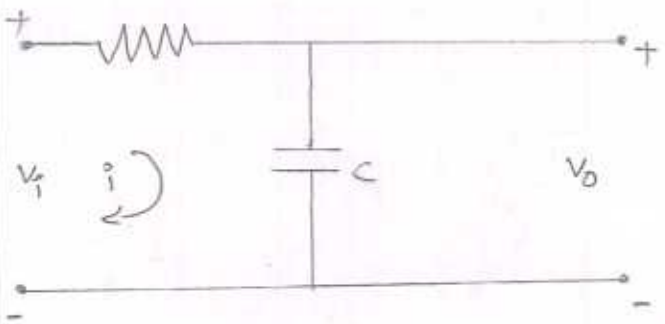
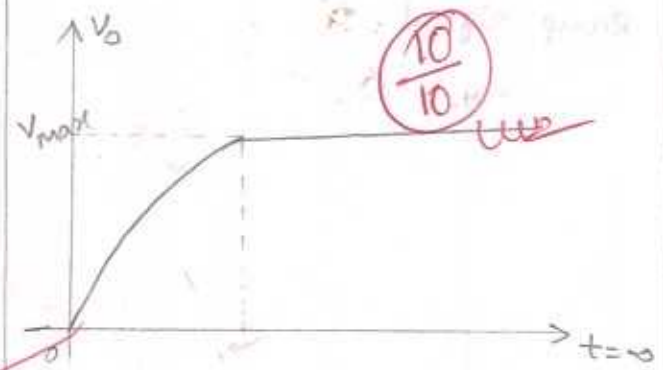
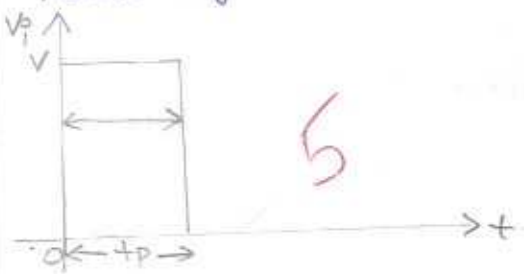
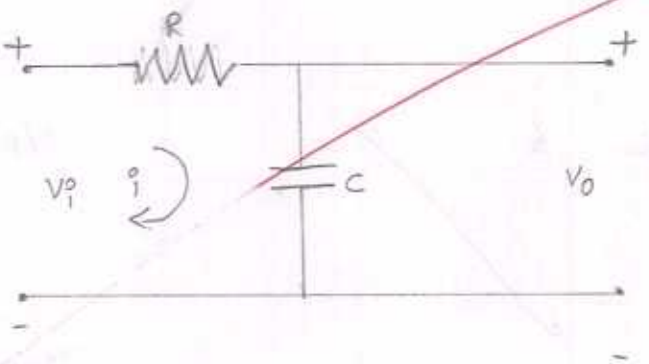
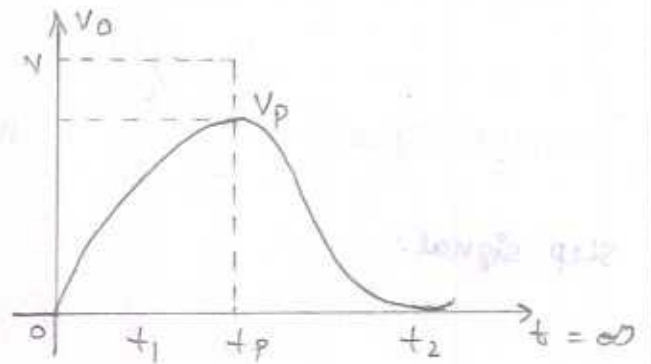
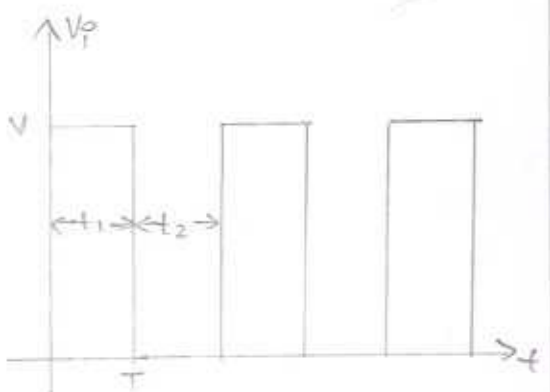
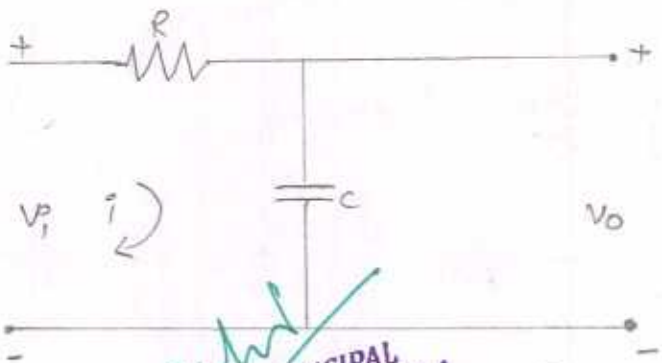
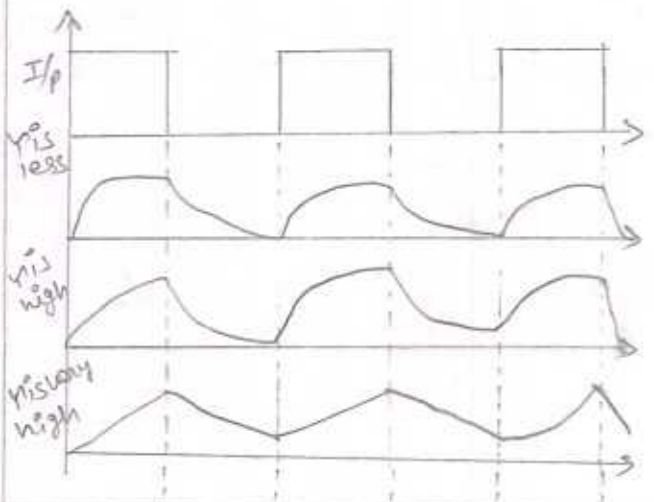
Figure 9.1 TTL NAND gate.

COPARISON OF LOGIC FAMILIES

Parameter	CMOS	TTL	ECL
Basic gate	NAND/NOR	NAND	OR/NOR
Fan-out	>50	10	25
Power per gate (mW)	1 @ 1 MHz	1 - 22	4 - 55
Noise immunity	Excellent	Very good	Good
t_{PD} (ns)	1 - 200	1.5 – 33	1 - 4



17TP1A0428. G.Vineesha. sub: PDC Unit Test - I

S.NO	Input signal	Circuit Diagram (LPRC)	output waveform
1	step signal 		 10/10
2	pulse signal 		
3	square signal 		

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Institute of Engineering & Technology,
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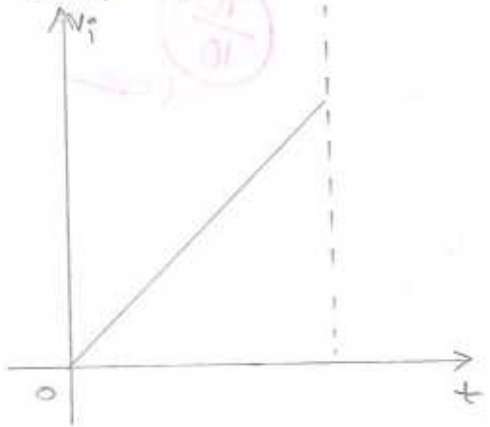
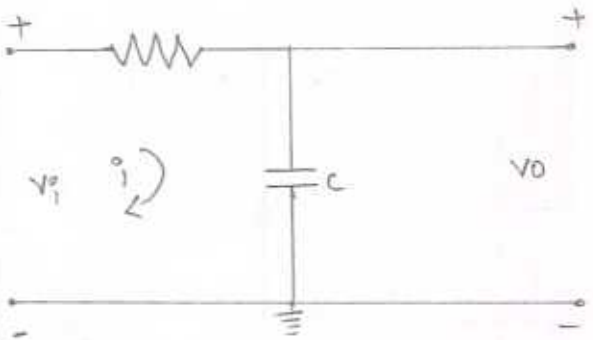
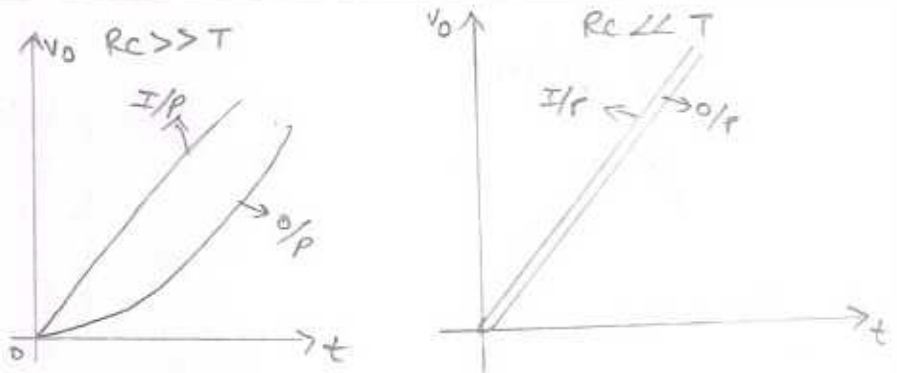
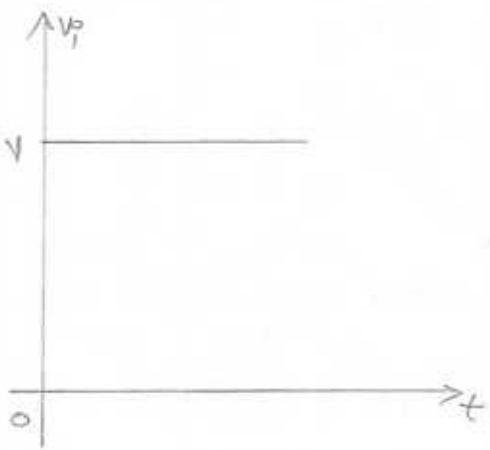
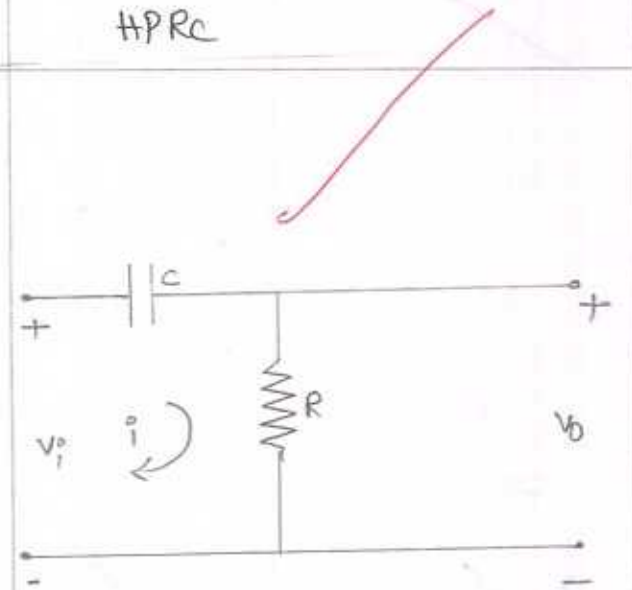
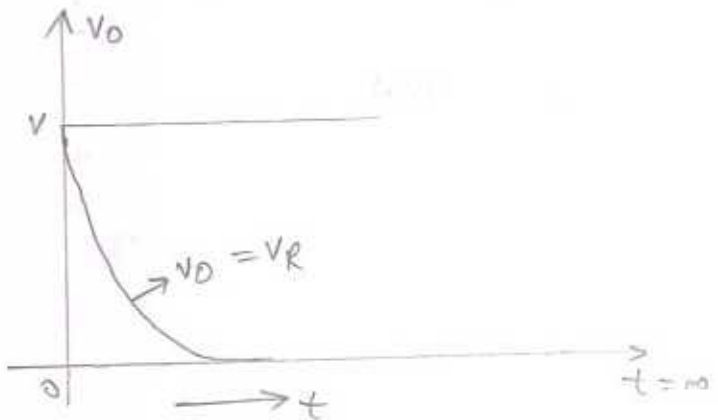
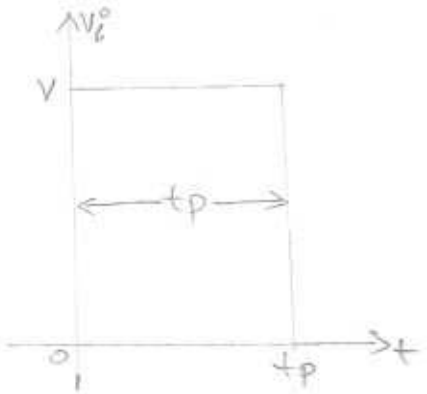
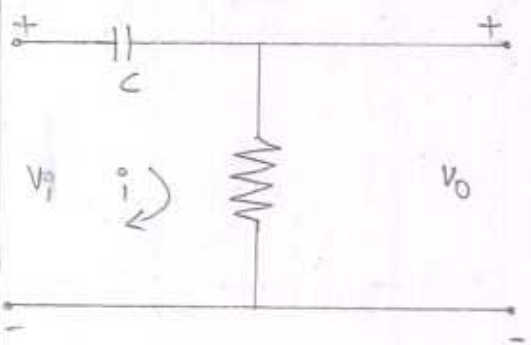
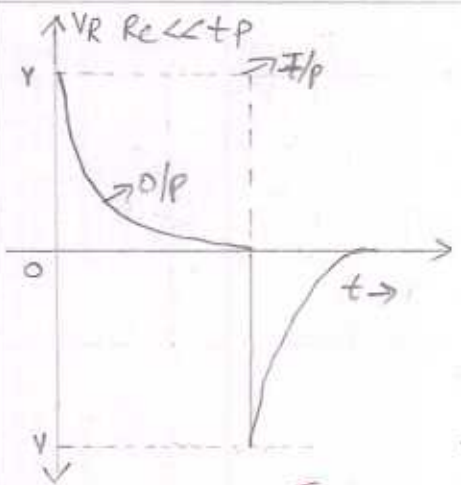
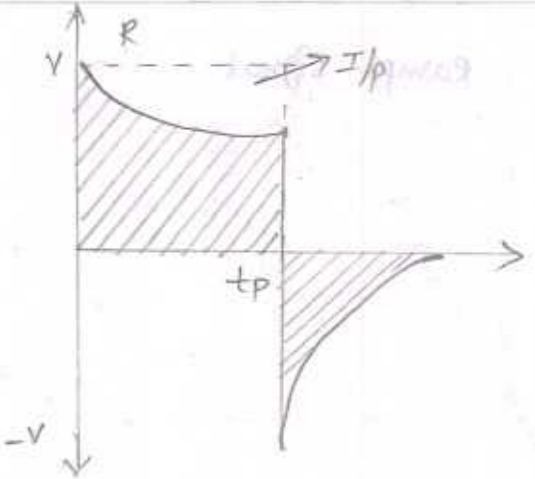
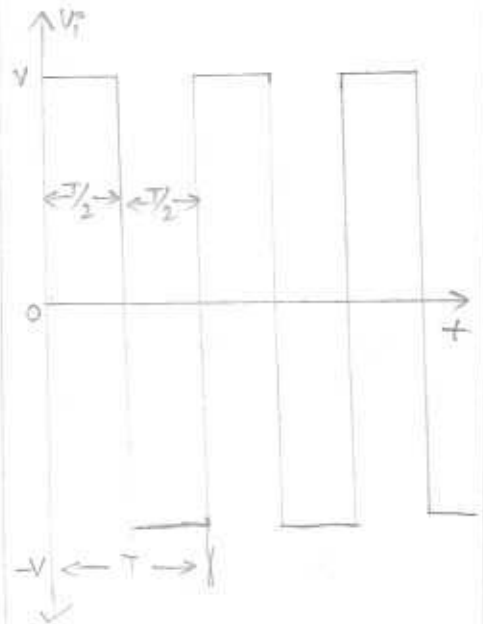
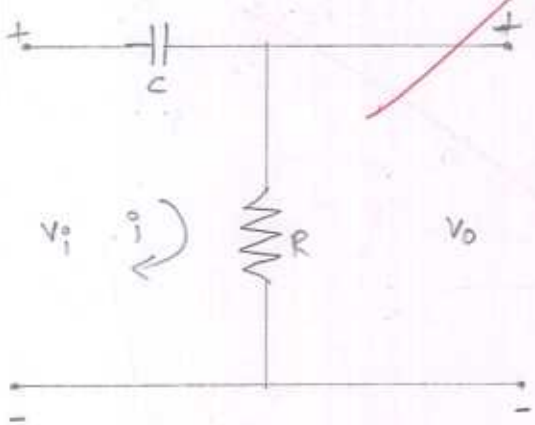
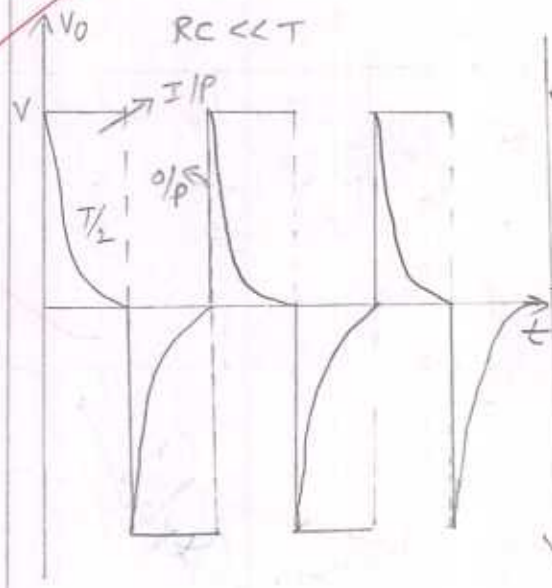
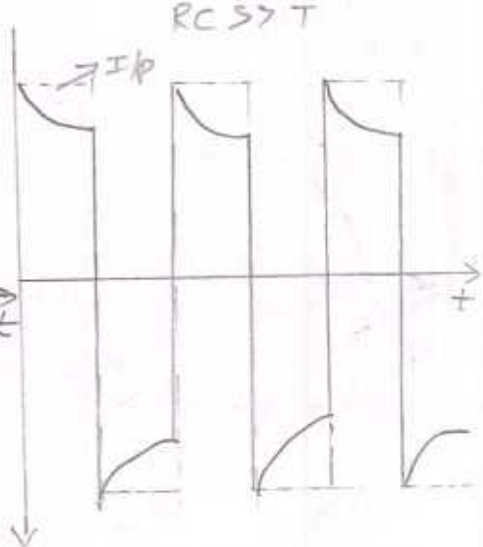
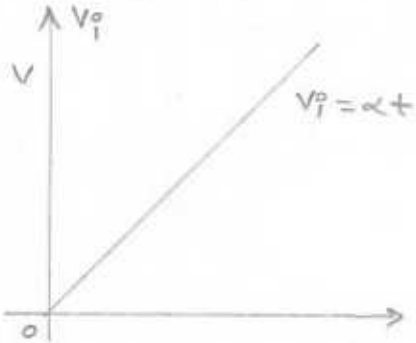
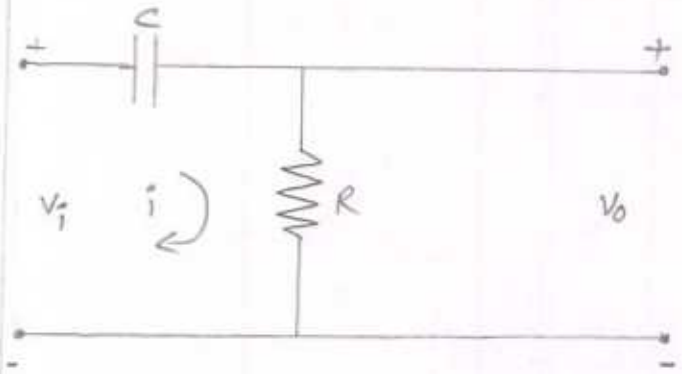
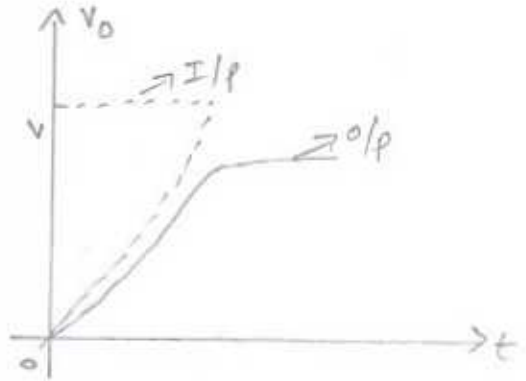
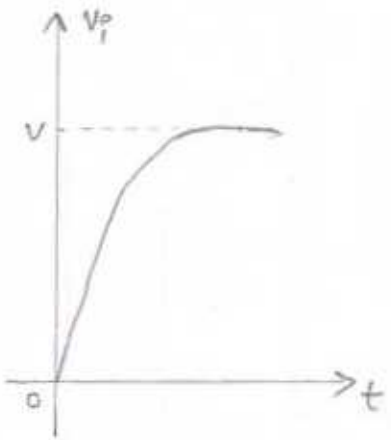
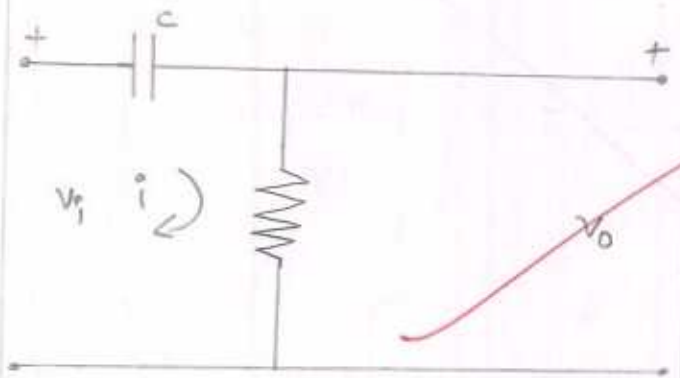
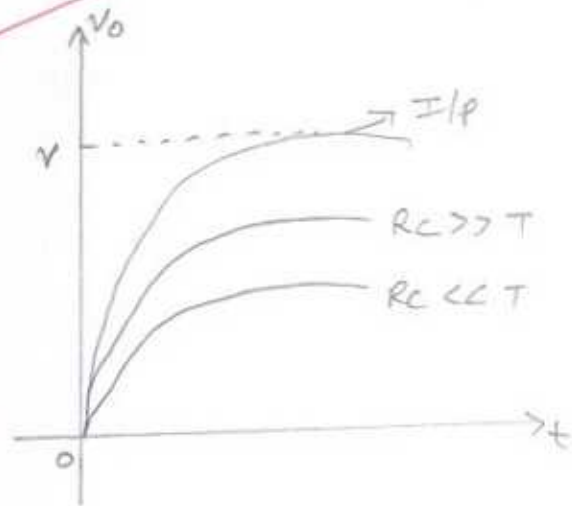
Input signal	circuit Diagram (LPRC)	output wave form.
4 Ramp signal 		

Input signal	HPRC	o/p wave form.
1 step signal. 		

I/p signal	HP RCkt	O/p wave form
2 pulse signal 		 
3) square signal 		 

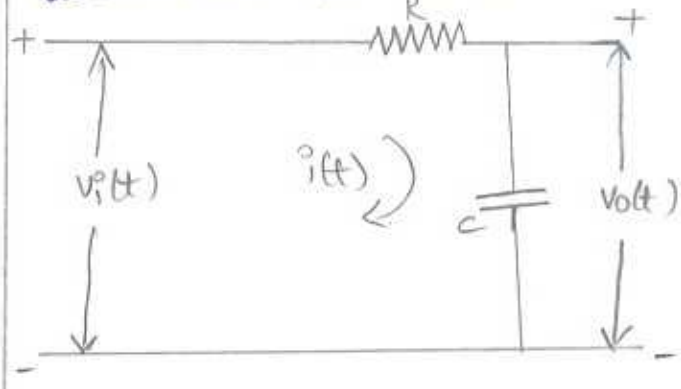
Input signal	HPRC	o/p wave form.
4 Ramp signal 		
5) Exponential signal 		

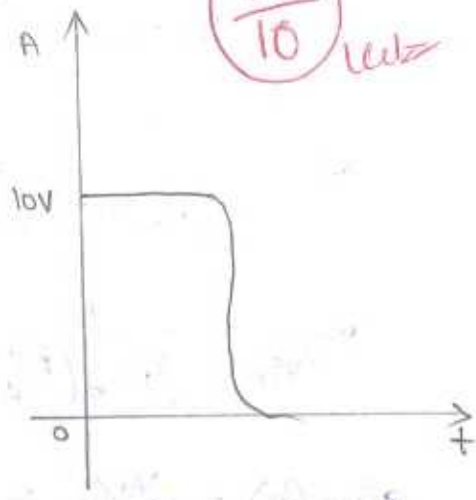
G. Vineesha 14111A0428, ECE, UNIT Test – 4

1) draw the o/p of the low pass RC circuit for different time constant to pulse i/p, square i/p?

10/10

* low pass RC circuit.





→ As above the circuit is low pass. ckt is only allows the low freeeny signal and attenuation high freeeny signal for low freeeny signal

$f=0 \quad x_c = \text{high (zero)} \uparrow \; ; \; x_c = \frac{1}{2\pi fC}$

→ for high freeeny signal

$f = \text{high} \quad x_c = \text{low (0)} \downarrow$

→ for low freeeny signal capacitor acts as open circuit so, we can measure the voltage across the capacitor

→ as freeeny is very low '0' we gets max. voltage and freeeny increase voltage decrease linearly

$V_D = IR \rightarrow (1)$

$I = \frac{V_{in}}{R_T} = \frac{V_{in}}{R - x_c}$

$I = V_{in} / R - 1/2\pi fC.$

$I = \frac{V_{in}}{R\left[1 - 1/2\pi fC\right]}$

PRINCIPAL
SIDDHARTHA
Institute of Engineering & Technology,
Vinobha Nagar(V), Ibrahimpatnam(M),
Ranga Reddy District-501 506.

$$I = \frac{V_{in}}{R\left[1 - j R_1/R\right]} \qquad R_1 = \frac{1}{2\pi f C}$$

$$V_o = \frac{V_{in}}{R\left[1 - j\left(R_1/R\right)\right]} \times R$$

$$V_o = \frac{V_{in}}{\left[1 - j\left(R_1/R\right)\right]}$$

$$V_o/V_{in} = \frac{1}{\left[1 - j\left(R_1/R\right)\right]}$$

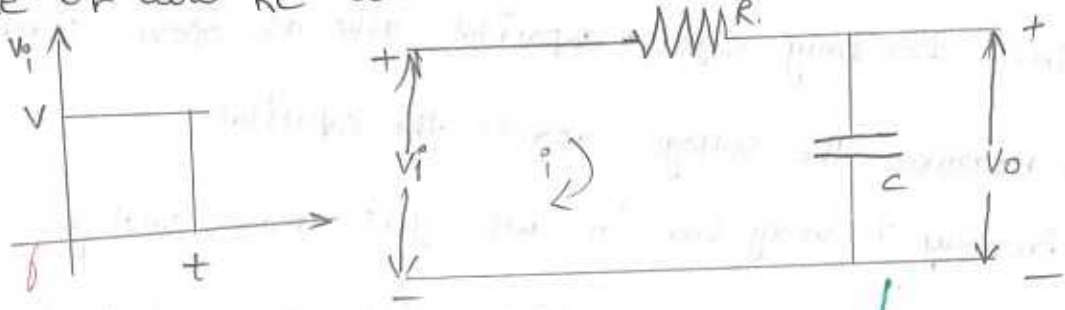
$$\text{gain } (A) = V_o/V_{in} = \frac{1}{\left[1 - j\left[R_1/R\right]\right]}$$

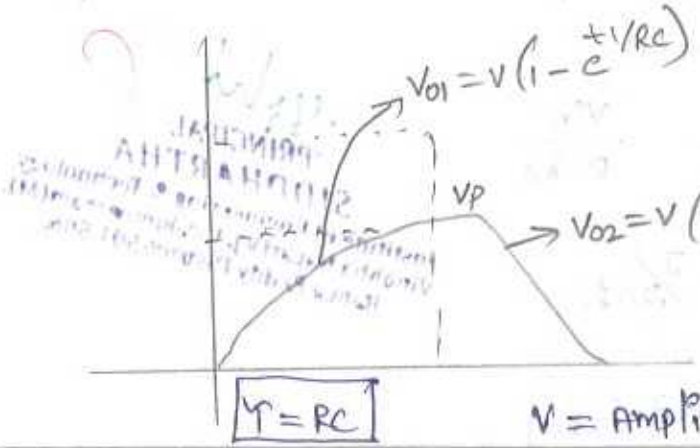
$$\left|V_o/V_{in}\right| = \frac{1}{\sqrt{1 + \left(R_1/R_2\right)^2}}$$

at $R_2 = R$.

$$\left|V_o/V_{in}\right| = \frac{1}{\sqrt{1+1}} = 1/\sqrt{2} = 0.707$$

* Response of low RC circuit for pulse i/p :—





V = Amplitude of i/p signal.

If the constant RC of ckt is very large at end of pulse 'V_0' is $V(1-e^{-t/RC})$ and o/p will decrease to zero from this

$$\boxed{\tau = RC}$$

it takes less time to charge is '$v_p < v$' $\tau = 20ms$ capacitor slowly charging

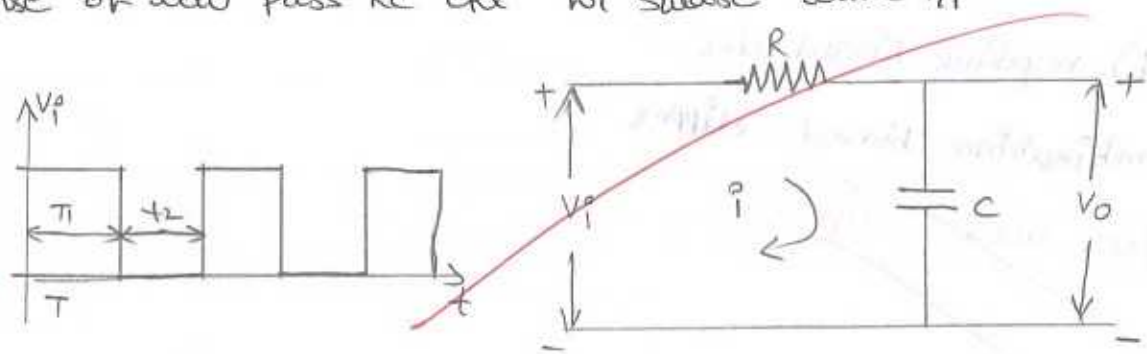
$$v_{01} = v\left(1 - e^{-t_1/RC}\right)$$

$$v_{02} = v\left(1 - e^{-t_2/RC}\right)$$

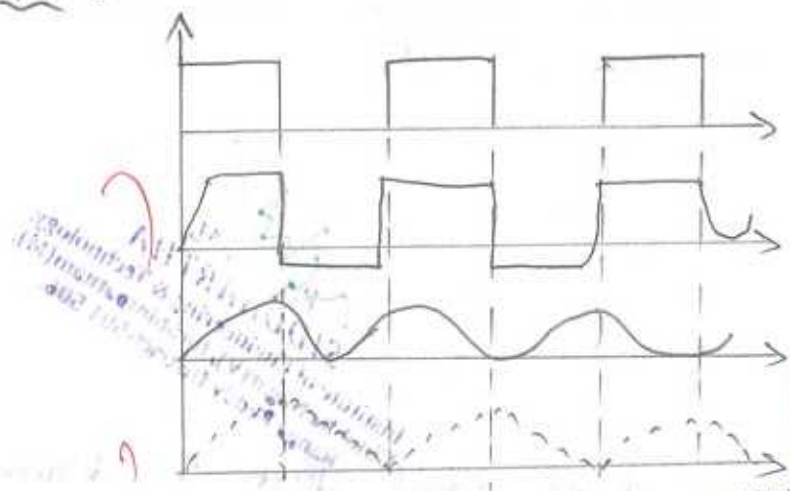
$$t_2 = t - t_p$$

$$v_{02} = v\left[1 - e^{-(t-t_p/RC)}\right]$$

Response of low pass RC ckt for square wave i/p



output :-



→ wave form which maintains itself at constant level V for a time T_1 and at other constant level '0' for a time T_2 and which is repetative with a period $T = T_1 + T_2$ is called square wave i/p.

classify different types of clipper circuit and explain their operation and also transistor characteristics?

clippers :— clipper is an electronic device which removes some portion of i/p signal either in positive half cycle negative half cycle.

→ clipper is a voltage limiter amplitude.

clipper types :—

→ positive diode clipper

→ negative diode clipper

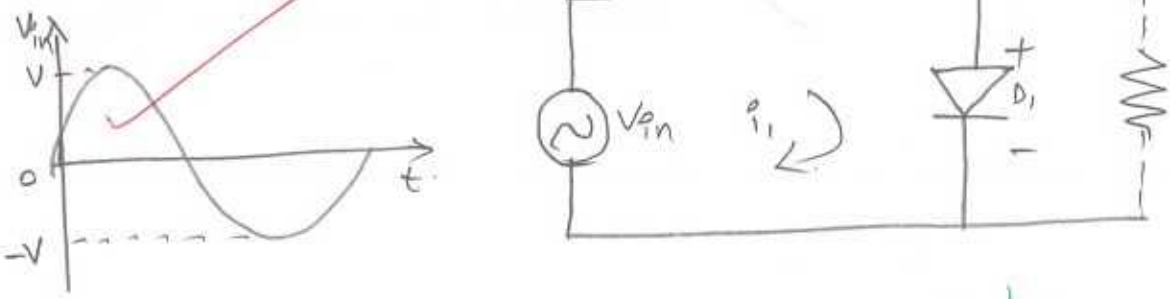
→ biased diode clipper

a) positive biased d.c

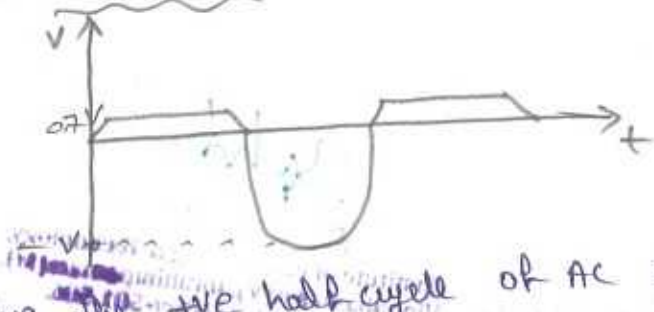
b) negative biased d.c

→ combination biased clipper

positive diode clipper :—



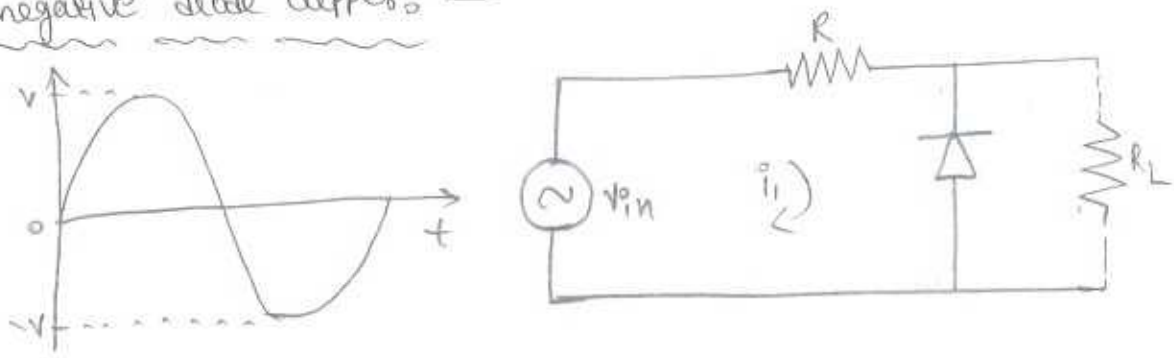
output waveform :—



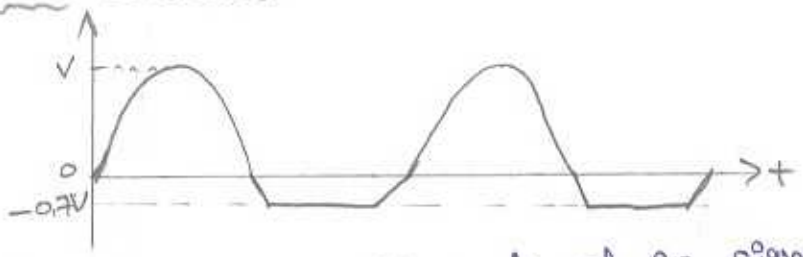
→ during the +ve half cycle of Ac signal diode is forward bias. during the '+ve' half cycle of Ac signal is reverse bias. current pass through the diode is after 0.7V

→ The o/p is same as the i/p signal.

3) negative diode clipper:—



output waveform:—



→ during the 'tve' half cycle of AC signal diode is reverse biase.

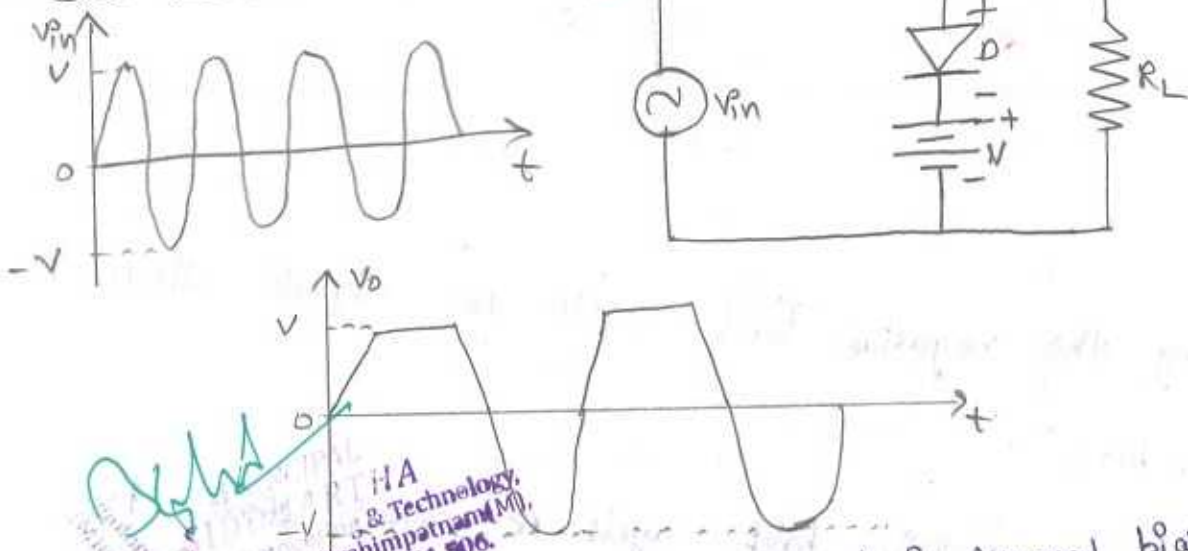
→ during the 've' half cycle of Ac signal diode is forward biase

→ current pass through the diode after 0.7V

→ The o/p is same as i/p signal.

*) biased diode clipper:—

a) 'tve' diode clipper:—



→ during the half cycle of AC signal is forward biase

→ 'v' bias voltage is acting as short circuit.

→ 0.7V as 0.7V is cut in voltage of silicon diode.

→ The output voltage will be equal to the cut in the voltage diode pulse voltage drop across V_{bias}.

→ i/p voltage always greater than the bias voltage.

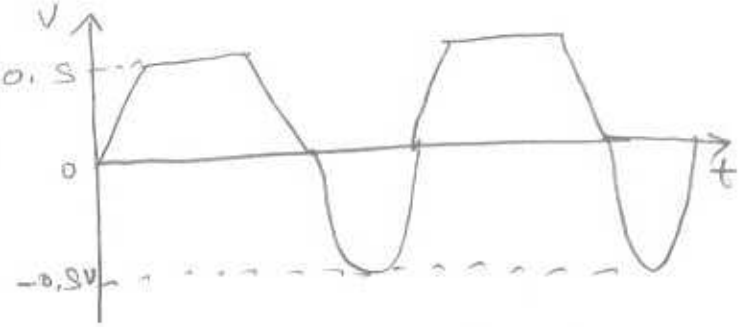
Ex:- $0.7V + 5 = 5.7V = V_o$

If $V_{bias} = 2V$ $V_{in} = 3V$

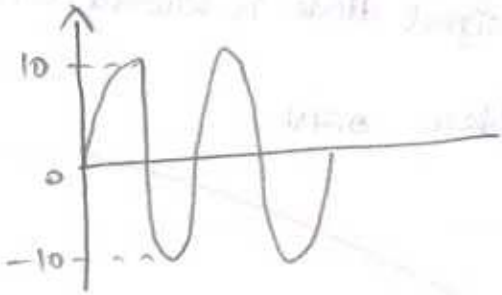
$V_o = 0.7V + V_{bias}$

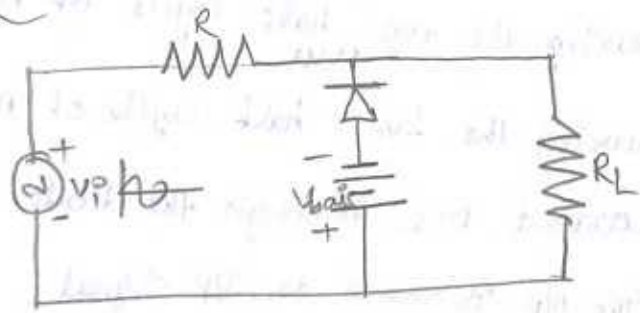
$V_o = 0.7V + 2V$

$V_o = 0.8V$

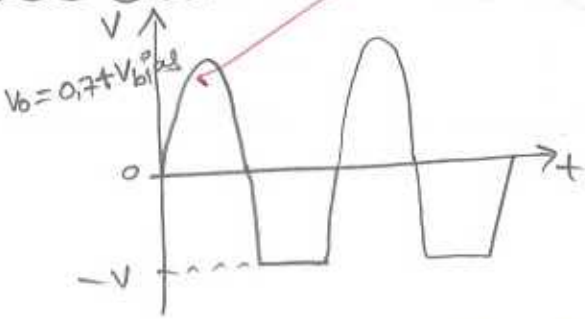


*) negative biased diode clipper :-





output waveform :-



→ during the negative half cycle Ac signal diode is forward bias

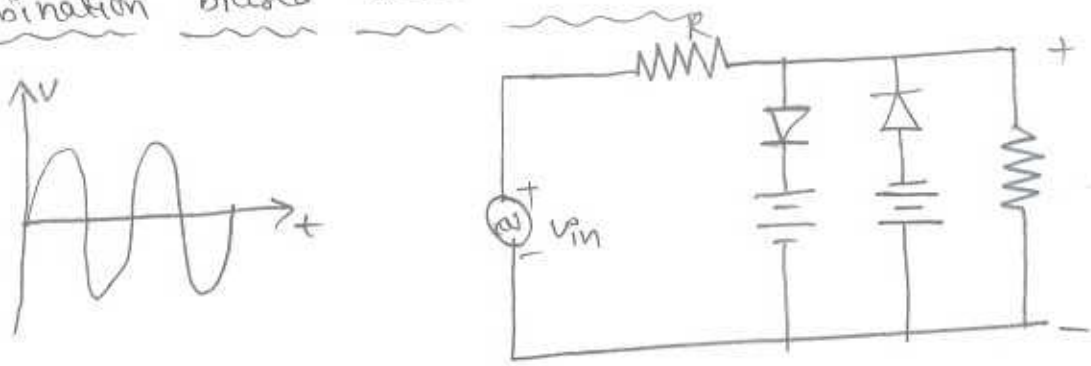
→ during the positive half cycle Ac signal diode is reverse bias.

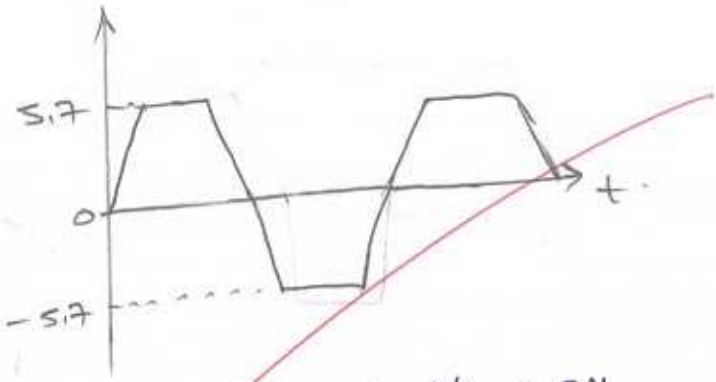
After from the 0.7V cut in voltage across the drop

→ Vout is equal to input signal.

→ It acting as a short ckt.

combination biased diode as clipper:—





$V_{in} = 10V,\ V_B = 5V,\ V_{B2} = 5V$

$V_o = 0.7 + V_{bias}$

$V_o = 0.7 + 5V$

$V_o = 5.7V$

$\boxed{V_o = 5.7V}$

1) Bi - directional sampling gate :-

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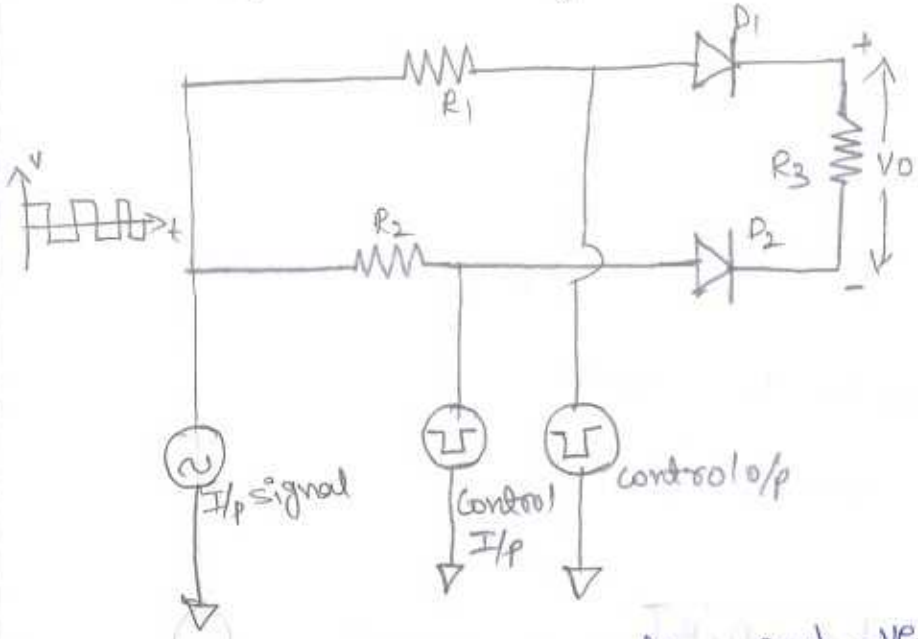
17PIA0428
PDC
UNIT Test-3



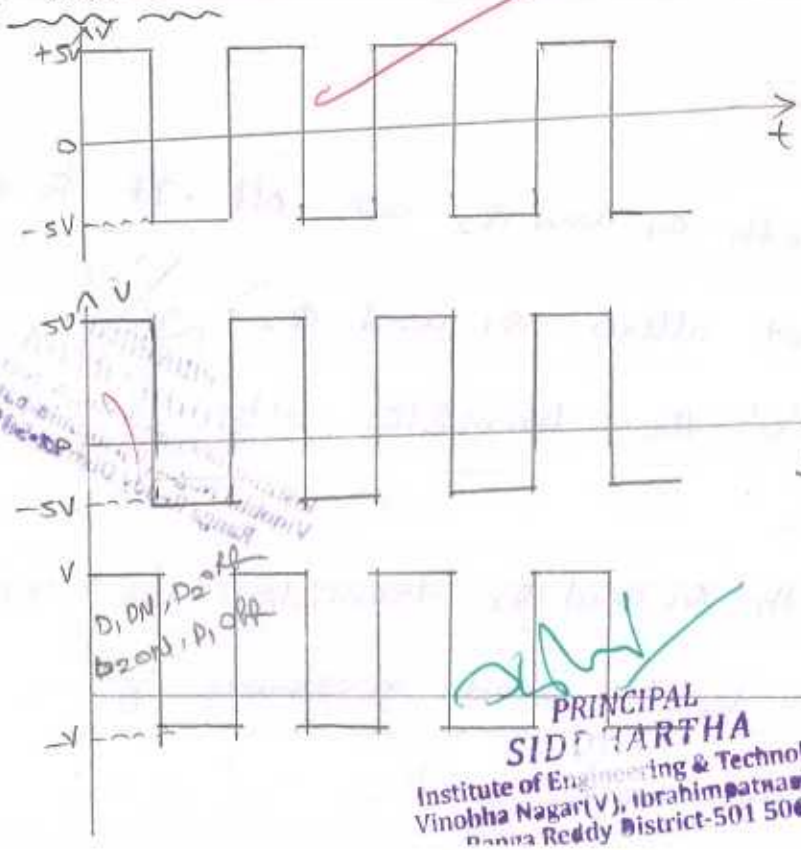
10/10

⇒ It produces the +ve waveform and -ve waveforms are continously. during the -ve low control I/p forward bias D_1 is off & D_2 is ON.

→ during the +ve high control I/p is forward bias, D_1 (diode) is ON and D_2 is OFF it pass through the resistance.

→ Bi - directional sampling gate is both (+ve) and (-ve) half cycle of the I/p signal.

output waveform :-



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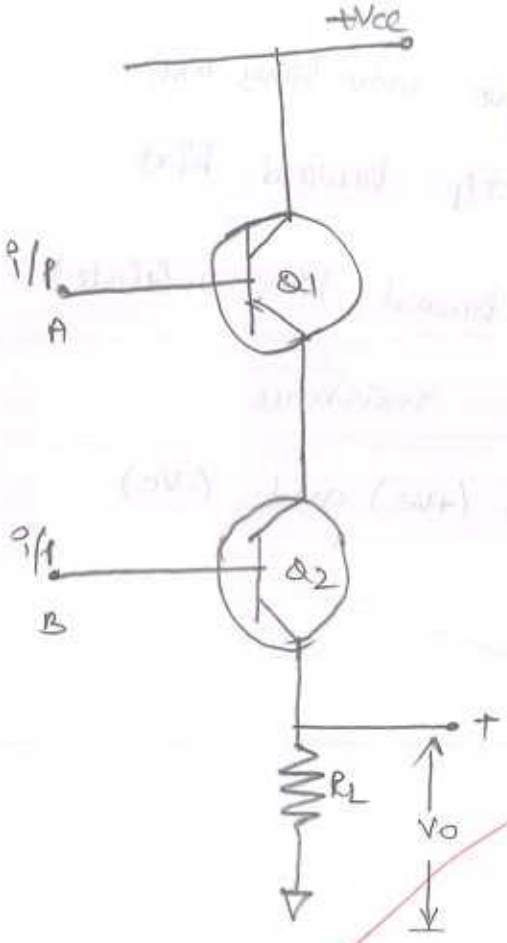
5) Realize the AND and OR gate using diode transistor.

AND gate is logic gate with multiple number of i/p's but only one output the output of AND gate is logic 1 (or) high only. If are the inputs are high else the output is zero.

→ '2' input AND gate using diodes the i/p' are indicated by 'A' and 'B' and 'Y' indicates the output.

Implementation of AND gate using transistor



$C = A \cdot B$

Truth table.

A	B	C=A.B
0	0	0
0	1	0
1	0	0
1	1	1

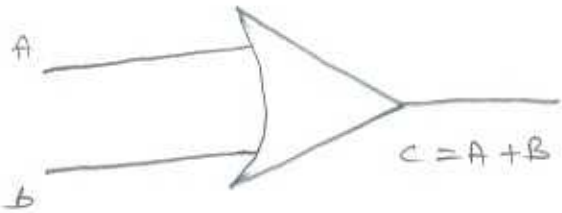
→ If A=0, B=0 both Q_1 and Q_2 are off. It is open ckt current does not allow Q_1 and Q_2 The o/p voltage is '0' the transistor acts in cut off region.

→ If A=1, B=1 both Q_1 and Q_2 transistor are 'ON' current passes from V_{cc} to load resistance 'R_L' and passes through ground output voltage 'V_o' is '1'.

Implementation of OR gate using diode :—

→ OR gate is an electronic device it can perform OR-operation b/w given operands.

logic symbol :—

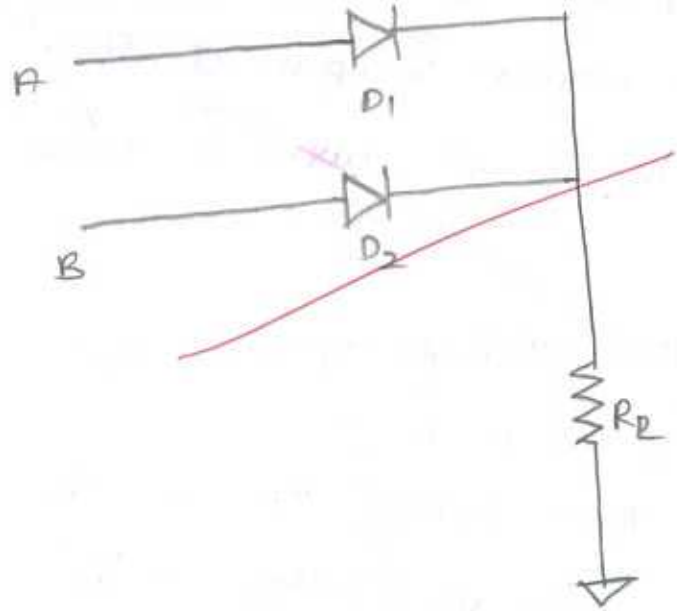


truth table :—

A	B	C = A+B
0	0	0
0	1	1
1	0	1
1	1	0

→ In OR gate operation both the i/p's are low then the o/p is high.

Implementation using diode :—

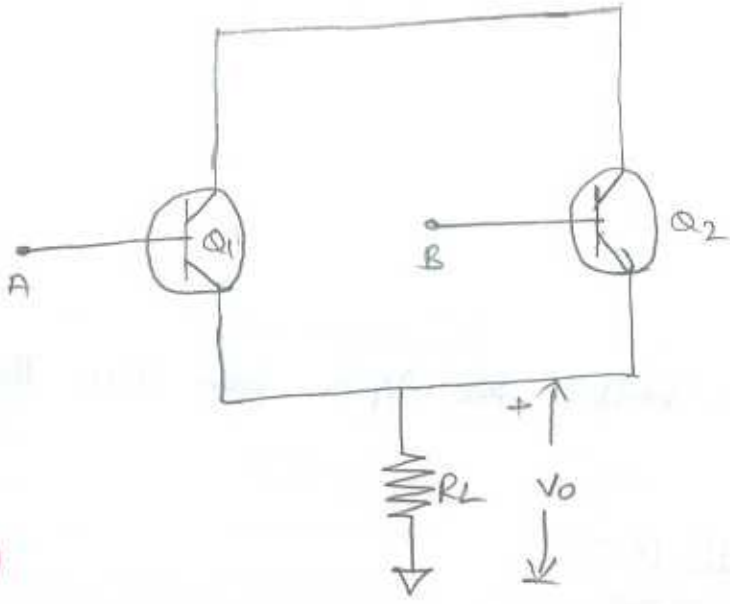


→ If we give i/p A=0, B=0 PN junction diode, is open circuit there is no current is passes. through D_1 and D_2 the o/p voltage V_o is '0'

→ If A=0, B=1, D_1 transistor is off But Q_2 transistor is ON and passes through load resistance 'R_L' o/p voltage 'V_o' is 1

→ If A=1, B=0 Passes through load Resistance 'RL' and o/p voltage Vo is 1.

Implementation of OR gate using transistor :—



→ If A=0, B=0 transistor Q1 and Q2 is off output voltage Vo is '0' A=0, B=0 current is open circuit

→ A=0, B=1 Q1 is off and Q2 is ON current passes through Q2 Vo is 1

→ If A=1, B=0 current Pass through Q1 and Q2 is on Q2 is off output voltage Vo is 1

→ If A=1, B=1 current passes through Q1 and Q2 both transistor are 'ON' Then the o/p voltage is 'Vo' is '0'

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10
10

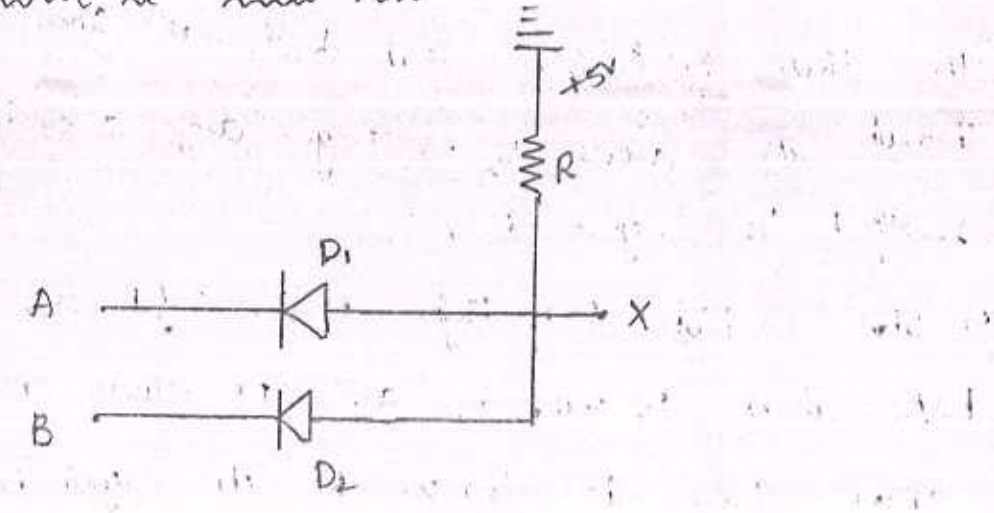
H.T. No. | 1 | 7 | T | P | 1 | A | 0 | 4 | 0 | 6 | Class/Yr/Branch: B.Tech. /M.Tech / M.B.A : II ECE

Mid Exam No.: 02 Subject: PDC

No. of Addl. Sheets: 01 Sign. of Invigilator: Date: 23/4/19

4) Realization AND gate and OR gate using diodes.

Realization of AND Gate :-



Two input logic Gate of AND Gate using diode

The above figure shows the two input logic Gate of AND Gate by using diode.

In positive logic Gate. Two inputs A and B are voltage source. and R is load resistance of a circuit. There is two diodes D_1 and D_2.

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(i) When A = low and B = low. both the inputs are
B=0 the Diodes D_1 and D_2 are ON. Current fl
through the resistor R. The output is x is 0.

(ii) when A = low and B = high A = 0 & B = +5V
the diode D_1 is ON and D_2 is OFF. Current flow
through the Diode D_1. voltage drop across the
resistor the output is x = 0.

(iii) when A = high and B = low A = +5V and B = 0V
the diode D_1 is OFF and D_2 is ON. Current flo
through the diode D_2. voltage drop across the
resistor R. the output is x = 0

(iv) when A = high & B = high A = +5V and B = +5V. the
both diods D_1 and D_2 are OFF. There is no
current flow the resistor R the output is x =

Truth table

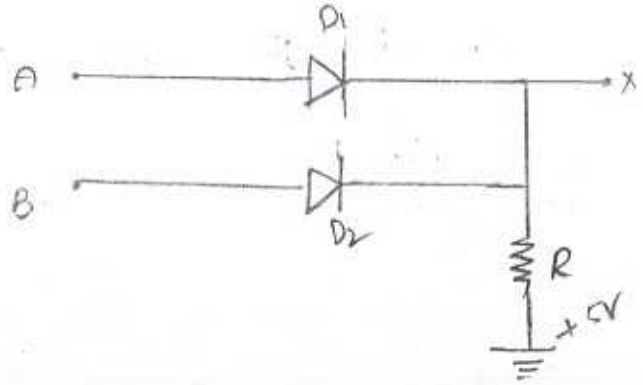
Input		O/p
A	B	x
Low	Low	Low
Low	high	Low
high	Low	Low
high	high	high

Truth table

Input		O/p
A	B	x
0	0	0
0	1	0
1	0	0
1	1	1

Truth table for

Realization of OR Gate :



Two input logic gate of OR Gate using Diodes

In positive logic Gate two inputs A and B are voltage source and R be the load resistance R. These two inputs produces the four possible combinations

i) When i/p A= low & B= low A = 0 & B = 0 the Diodes D_1 and D_2 are OFF. There is no current flow Through the resistor R. The output of x is zero

ii) When i/p A= low & B= high A = 0 & B = +5V The Diode D_1 is off and D_2 is ON. there is D_2 is current flow through the resistor R. The output of x is high

iii) when i/p A= high & B= low and B = 0 the Diode D_1 is ON, and D_2 Diode D_1 is Current flow through the resistor R. The output of

iv) when i/p A = high & B = high A = +5V & B = +5V

Both the Diodes D_1 and D_2 are ON. There is a current flow through the resistor. Then the output of x is high.

Truth table

Input		o/p
A	B	x
Low	Low	Low
Low	high	high
high	low	high
high	high	high

truth table

Input		o/p
A	B	x
0	0	0
0	1	1
1	0	1
1	1	1

Truth table for OR Gate

2) Transistor Miller Time Base Generator

Transistor miller time base Generator consist of a three stage amplifier. Q_1 Q_2 Q_3 first stage of amplifier is common Emitter follower. It reduces the high input impedance

Third stage of amplifier is Emitter follower by the two reasons.

first reason. There is low resistance of impedance R_0 is reduces the load resistance drives

Second is the high input impedance produces the less resistance drives.

The third stage of amplifier is connected to the Our transistor.

There is a capacitor of by pass capacitor which is the diode there is a capacitor charges.

Q_1 is OFF then the capacitor is prevent the charging there is a Emitter follower

By using Schmitt trigger the o/p voltage is trigger to the resistance it gives the wave form the coupling capacitor acts to the charge to the

$V_s = \frac{V_i}{r}\left[1 - \right.$

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II B.Tech. II Sem., IInd Mid-Term Examinations, April – 2019

Branch: ECE **Subject: PDC**

Date: 23-04-19-AN **Objective Exam** **Time: 30min**

Name: A. Nagaroni **Hall Ticket No.** 17TP1A0406.

Answer All Questions. All Questions Carry Equal Marks. Time: 30 Min. Marks: 10.

10/10

I. Choose the correct alternative:

1. Which of the following logic family has highest fan-out? (D)
   A) ECL B) TTL C) DTL D) CMOS
2. A sinusoidal waveform can be converted to a square waveform by using _____ (C)
   A) Astable multivibrator B) Bitable multivibrator C) Schmitt trigger D) None of the above
3. In Miller time base generator, which of the following is used (B)
   A) An inverting amplifier with a gain of unity B) an inverting amplifier with a gain of infinity
   C) Non-inverting amplifier with a gain of unity D) non-inverting amplifier with a gain of infinity
4. Bootstrap's sweep circuit produces _____ type of waveform. (B)
   A) Positive going Ramp B) negative going Ramp C) either A or B D) Both A and B
5. Circuit which consist of a quasi-stable state is called (B)
   A) Bistable circuit B) nonstable circuit C) tri stable circuits D) tristate circuit
6. To get a saw-tooth output waveform, the restoration time is (A)
   A) Zero B) rise time C) storage time D) infinity
7. Bootstrap's sweep circuit produces _____ type of waveform. (B)
   A) Positive going Ramp B) negative going Ramp C) either A or B D) Both A and B
8. Applications of time base generator (C)
   A) Multivibrator B) logic gates C) CRO D) A & B
9. Multivibrator has how many states? (C)
   A) 0 B) 1 C) 2 D) 4
10. Transistor saturation region operation in the following biase (D)
    A) R.B, R.B B) R.B, F.B C) F.B, F.B D) F.B, R.B

I. Fill in the Blanks

11. A time base generates is an electronic circuit which generates an output voltage or current waveform.
12. The No of quasi stable states of mono stable is 01
13. When the diode is forward biased it acts as short circuit (SC)
14. The basic TTL gate is AND Gate
15. Schmitt trigger is a Emitter Coupled bistable multivibrator
16. Which is the best logic family in bipolar technology TTL
17. Which logic gate having high fan-out CMOS
18. Define sampling gate Output waveform reduces the same input @ time interval
19. Transistor saturation voltage in ON configuration 0.1 – 0.3v Circuit switch
20. Draw any RTL logic gate

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INTERNAL EXAMS ANSWER BOOK

16
10

H.T. No. | 1 | 7 | T | P | 1 | A | 0 | 4 | 0 | 6 | Class/Yr/Branch: B.Tech. /M.Tech / M.B.A : II year ECE

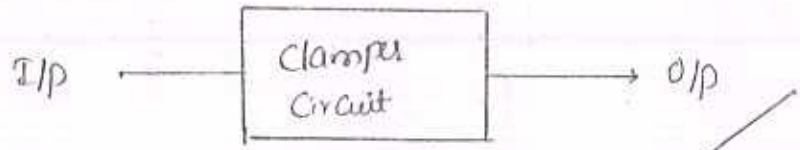
Mid Exam No. : 01 Subject : PDC

No. of Addl. Sheets : 02 Sign. of Invigilator : Date : 19/2/19

4) Clamper :-

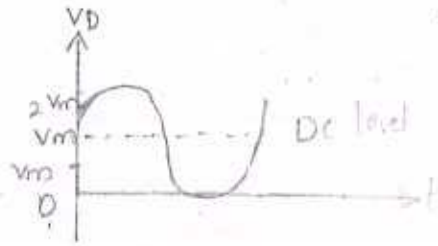
Clamper is a non linear Electronic device 'dc' level is a input signal. It adds 'dc' level is a input signal.

Block diagram of clamper.



Block diagram of clamper circuit

output wave form of clamper circuit



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Biased clamper

In biased voltage is series with the Diode then

with in a dc level voltage. which is required be dc level is 1% to 99% will be occured.

Biased clampers:

Biased clampers are four types

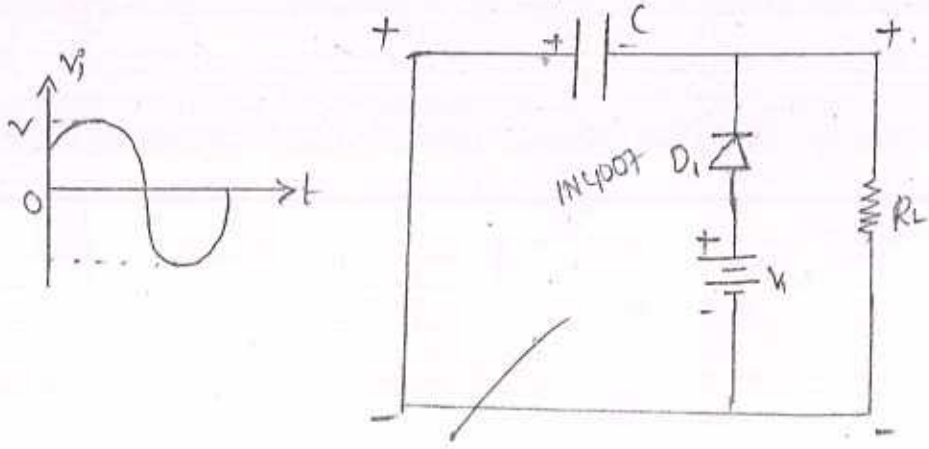
1) positive clamper with positive Bias

2) positive clamper with negative bias

3) positive negative clamper with positive bias

4) Negative clamper with negative bias.

* positive clamper with positive Bias



V_1 Biased voltage is series with diode D_1 then the Circuit is biased clampler.

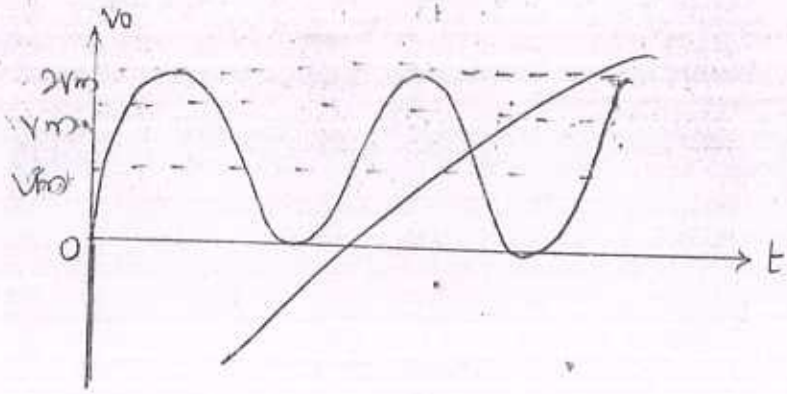
In these Circuit D_1 is diode, V_1 is voltage (Biasing) C is Capacital. R_L is load resistance.

* During positive half cycle of an input Ac

Its acts as an short circuit. Capacitor is charged.

* During negative half cycle of an input Ac signal. Diode D is Reverse biase. Then the circuit acts as open circuit. Kapacitor is discharged.

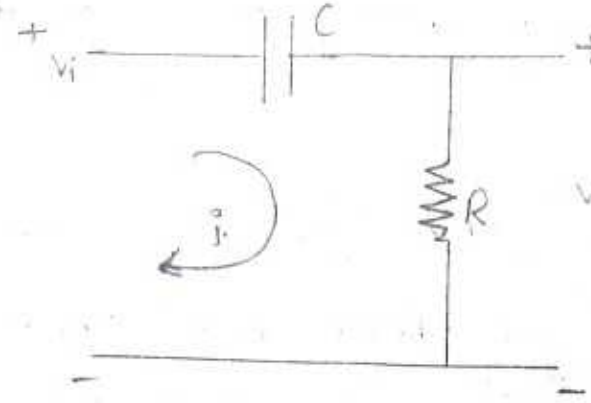
Output wave form:



2) Operation of high pass RC Circuit for Square wave input signal.

* High pass RC Circuit.

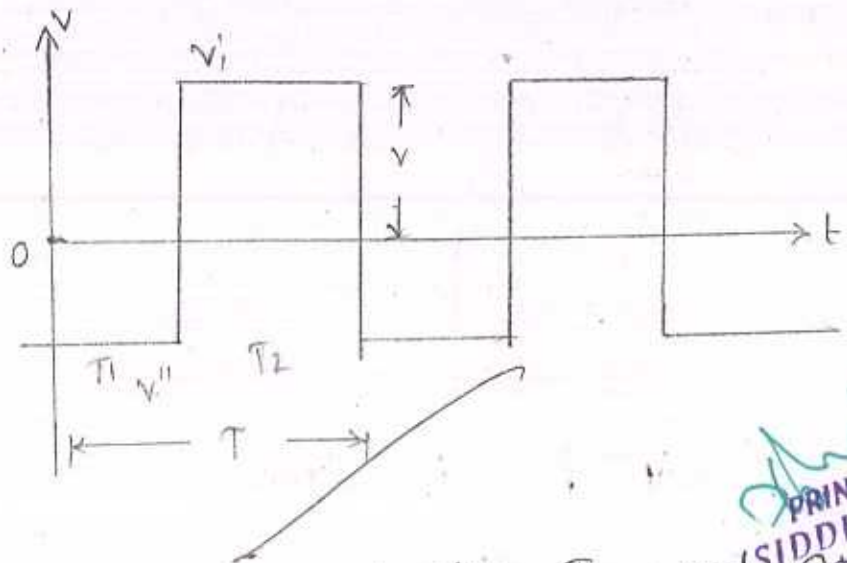
High pass RC Circuit, which passes the high frequency signal. It attenuates the low frequency signal. It is called high pass RC Circuit



High pass RC Circuit.

Square wave input signal:

Square wave is a combination of two positive and negative step signals



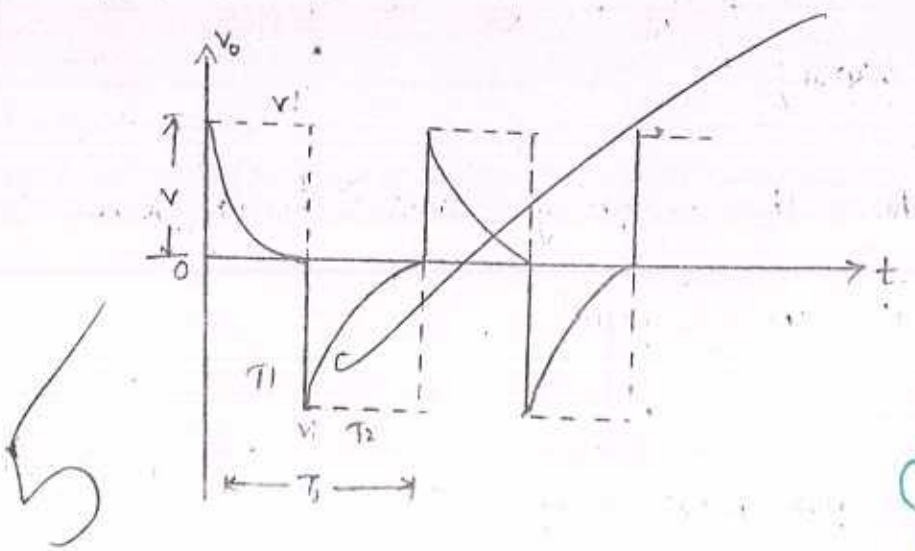
V_i' is the level of time T_1 and another V_i'' is the level of time T_2. There is adds of combined the time T_1 and T_2 is called time period

These Square wave input signal is applied to the high pass RC Circuit.

* The response of high pass RC Circuit is depends upon the time Constant. RC components

(i) $RC << T$

Output response of high pass RC Circuit

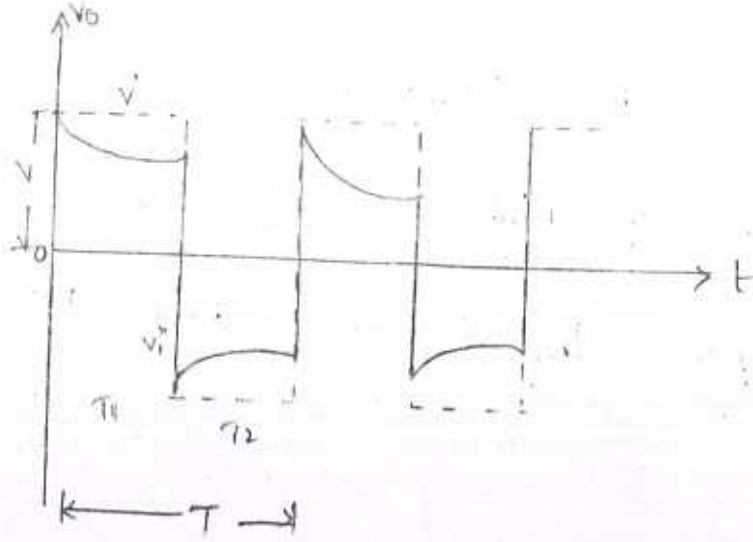


At $t = 0$ then the frequency increase the o/p value rises to the peak of the signal

At $t = \infty$ then the frequency decrease the output value suddenly changes to the down the signal.

(ii) $RC >> T$

Output response of high pass RC circuit



At $t=0$ then frequency increase the o/p it varies to peak of signal

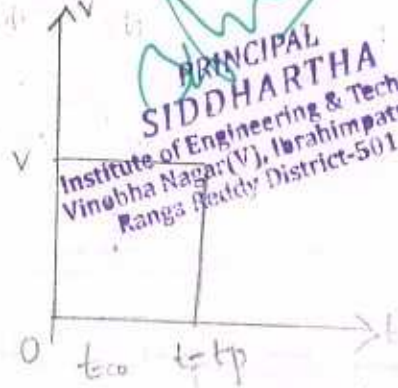
At $t=\infty$ then the frequency decrease the o/p values fall down the signal.

1) Pulse input (Pulse input is given to the low pass RC circuit)

Mathematical representation

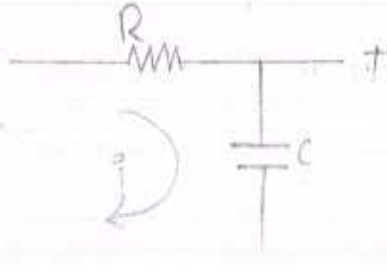
$V_1(t) = 0$ for $t<0$ & $t>t_p$

$= V$ for $0<t\leq t_p$

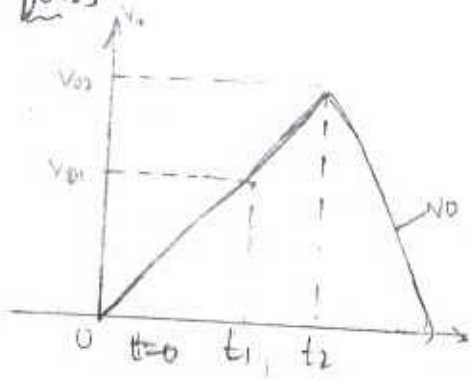


Low pass RC circuit

It allows low frequency signal. It attenuates high frequency



output wave forms



Ideal pulse signal is +ve and -ve values

$$v_{o1}(t) = v(1 - e^{-t/RC})$$

$$v_{o2}(t) = v(1 - e^{-t/RC})$$

$$t_2 = t - t_p$$

$$\boxed{v_{o2}(t) = v\left(1 - e^{(t-t_p)/RC}\right)}$$

At $t=0$ frequency increases the capacitor is low

At $t=\infty$ frequency decreases the capacitor is high

the output will be rise and suddenly fall to the down.

Step input signal:

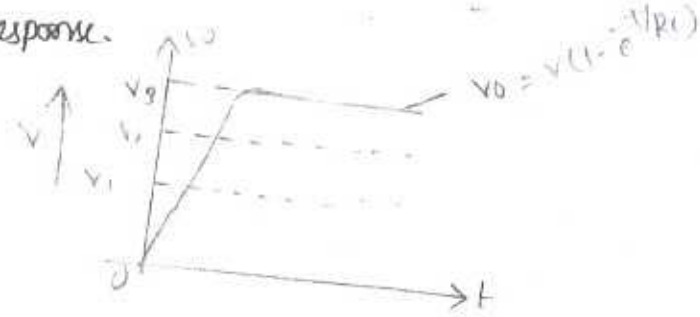
Mathematical representation

$v(t) = v \quad t<0$ or $t>0$

$= 0$ Elsewhere

Step input signal is given to the low pass RC circuit the output response is depends on time constant

output response.



At $t \geq 0$

$$iR + \frac{1}{C}\int i\,dt = v_i$$

differentiate

$$\frac{di}{dt}R + \frac{1}{C}i = v$$

divide with R

$$\frac{di}{dt} + \frac{1}{RC}i = \frac{v}{R}$$

$$\frac{di}{dt} + \frac{1}{RC}i = i$$

$$\boxed{i = k_1 e^{-t/RC}}$$

At $t=0$

$$i = \frac{V}{R}$$

$$i = k_1 e^{0/RC}$$

$$\boxed{\frac{V}{R} = k_1} \Rightarrow i = \frac{V}{R} e^{-t/RC}$$

By the output voltag $v_0 = V - iR \Rightarrow v_0 = V - \frac{V}{R} e^{-t/RC} \cdot R$

$$= V(1 - e^{-t/RC})$$

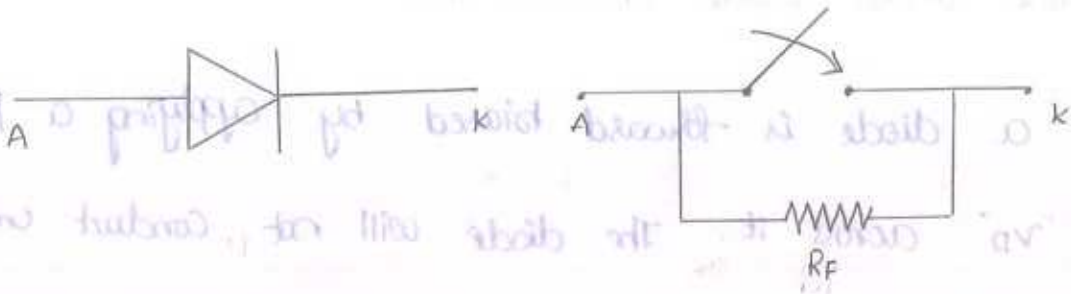
$$v_0 = V(1 - e^{-t/RC})$$

* Switching Characteristics of Devices. *

3.1 Diode as a switch

The diode acts as a switch, when it gets ON for forward biasing and OFF for Reverse biasing

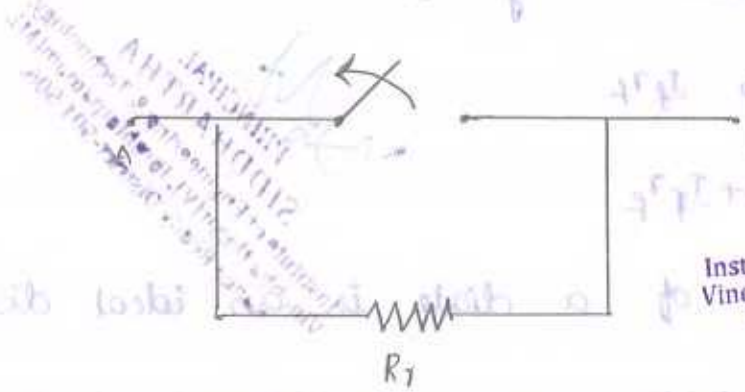
a diode as a closed switch



when the diode is forward biased. i.e. the potential at anode A is greater than Cathode K. the switch gets closed. The voltage and resistance between anode and Cathode becomes ideally zero.

the forward resistance R_F of diode is typically of a few ohms

the diode as an open switch



when the diode is reverse biased ie. the potential at

Anode A is Cathode k, the switch gets open. Ideally, the current is zero and resistance is infinite.

the reverse resistance R_r of diode is typically of few mega ohms.

3.2 Piecewise linear Diode characteristics

when a diode is forward biased by applying a positive voltage 'v_D' across it. The diode will not conduct until the applied voltage 'v_D' is greater than the potential barrier voltage 'v_0' at the junction. while conducting the current, I_f flowing through the diode causes a voltage drop due to its forward resistance 'r_f'. Thus the forward voltage v_D applied across the diode has to overcome.

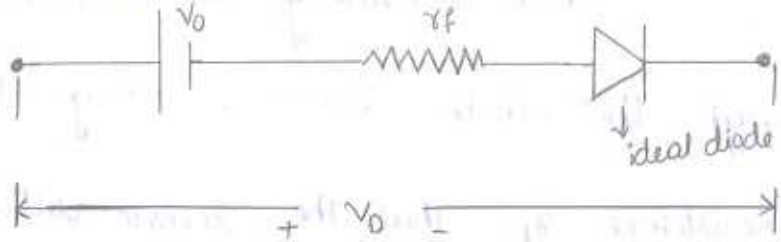
a) potential barrier voltage v_0.

b) voltage drop. $I_f r_f$

$\therefore v_D = v_0 + I_f r_f$

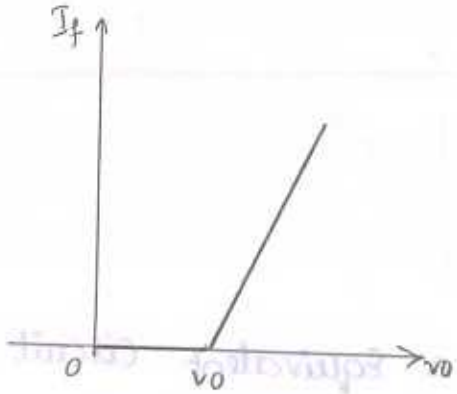
Hence equivalent of a diode is ideal diode in series with a battery v_0 and internal resistance r_f

as shown in figure



fig(a) Equivalent Circuit of piece wise linear model.

The V-I characteristics of the Equivalent Circuit in figure (a) is as shown in figure (b). Since the characteristics are linear piece wise it is called piece wise linear model. Further, the V-I characteristics in figure (b) are approximately equivalent to the original V-I characteristics of PN diode. Hence the model is also known as approximate Equivalent Circuit model.



fig(b). V-I characteristics of piece wise linear model

when a diode is reverse biased by applying a negative voltage 'V' across it. The diode will not conduct until the

applied voltage v_D is less than the potential barrier voltage v_0 at the junction while conducting the current I_f flowing through the diode causes a voltage drop due to its reverse resistance 'r_f'. Thus the reverse voltage 'v_D' applied across the diode has to overcome.

a) potential barrier voltage v_0

b) voltage drop, $I_f r_f$

$$\therefore v_D = v_0 + I_f r_f$$

Hence Equivalent Circuit of a diode is an ideal diode is in series with a battery v_0 and internal resistance r_f as shown in fig (a)

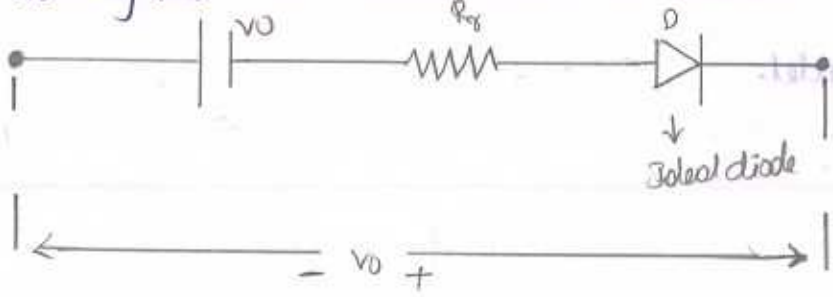
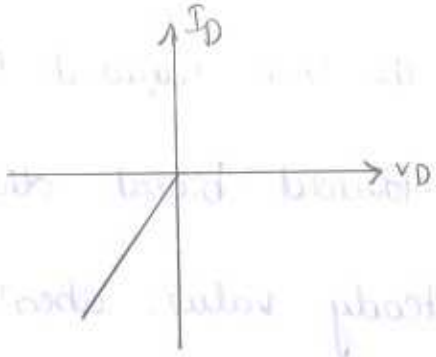


fig (a) Equivalent Circuit for piece wise linear model

The V-I characteristics of a Equivalent Circuit in fig(a) as shown in fig (b). Since the characteristics are linear piece wise, it is called piece wise linear model. Further the V-I characteristics in fig(b). are approximately Equivalent to the original V-I characteristics of PN diode.

Hence, the model is also known as approximate Equivalent Circuit model.



fig(b) V-I characteristics of piece wise linear model.

3.3 Diode switching times.

The accumulation of charge in forward bias and depletion of charge in reverse bias donot allow the semiconductor diode to make abrupt ON-to-OFF and OFF-to-ON transitions. As these transitions involve transitions. The diode cannot respond immediately to sudden changes occuring in the Externally applied voltage.

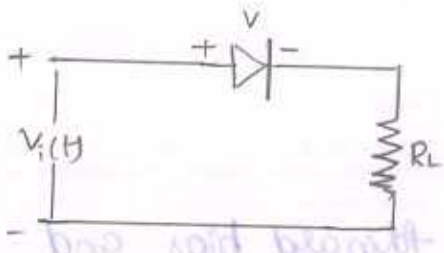
Forward recovery time.

It is defined as the time required for the current flowing through a reverse biased diode to reverse and attain a steady value. when a forward bias

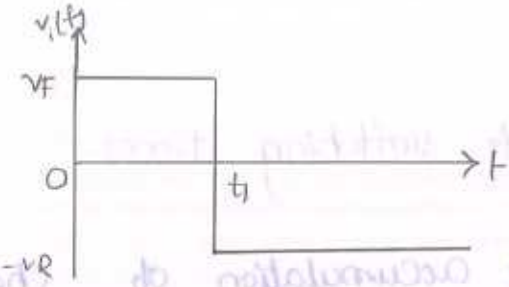
is applied to it suddenly.

Reverse recovery time.

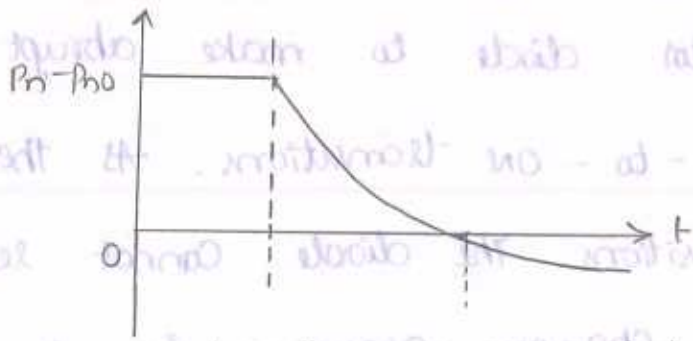
It is defined as the time required for the current flowing through a forward biased diode to reverse and attain a steady value. when a reverse bias is applied to it suddenly.



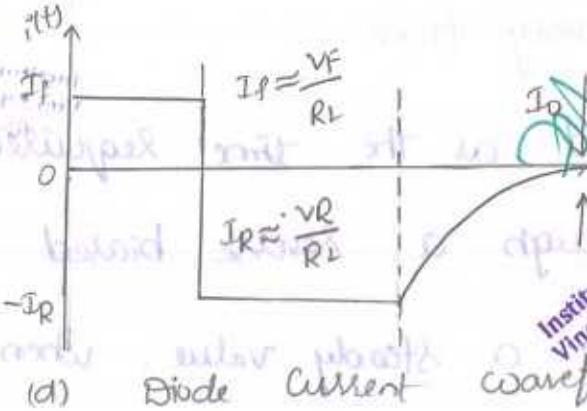
(a) The diode circuit with R_L



(b) The negative i/p waveform.



(c) The Excess carrier concentration at the p-n junction



(d) Diode Current waveform

(e) diode voltage waveform.

The storage and transition times of a diode

Consider the Cucuit as shown in fig (a). containing a diode with a load resistance R_L. Let us assume that this diode is initially ON, that is in the steady state forward bias condition. The input signal that is applied to this circuit is shown in fig (b). The input voltage V_F almost appers across the load resistance R_L.

Then the diode current $i = I_f \simeq V_F/R_L$. TO take the diode into OFF state. This input voltage to the Circuit V_i is abruptly reversed from V_F to $-V_R$. At the time of this reversal in the diode state, current does not become zero. Instead the diode current reverses and remains at $I_R = -V_R/R_L$. for a duration is known as the storage time. /OR.

PRINCIPAL
SIDDHARTHA
Institute of Engineering & Technology.
Vinobha Nagar(V), Ibrahimpatnam(M),
Ranga Reddy District-501 506.

3.3.1 Storage time

when reverse bias is applied suddenly to diode operating in forward bias condition. A certain time is required for the stored minority carriers on either side of the junction to move into other side and become majority carriers. the time required for this process is known as storage time.

3.3.2 Transition time.

The time interval in the which the reverse current decreases Exponentially and becomes Equal to I_S (Reverse saturation Current), when a forward biased diode is reverse biased suddenly. is known as transition time t_t.

The reverse recovery recovery time t_{rr} is the sum of the storage time and the transition time. The variation of the input voltage during reverse recovery is shown along with the diode current in fig (d).

In fig (e) we can see the variation of stored majority charge Concentration and diode voltage.

3.4 Transistor as a Switch

The transistor acts as a switch when it is placed in series with the load and supply voltage. The External signal drives the transistor between cut-off and saturation and it produces the desired waveforms. one of the main applications of transistors are solid state switches. Generally solid state switches are used to control high power devices like motor, solenoids. and digital circuits.

For switching application transistor must be operated in saturation and cut-off regions. For brief explanation of transistor switch consider the common Emitter configuration i.e as shown in fig (1). The CE amplifier circuit consists of R_B, R_C and it gives the output with 180° out of phase.

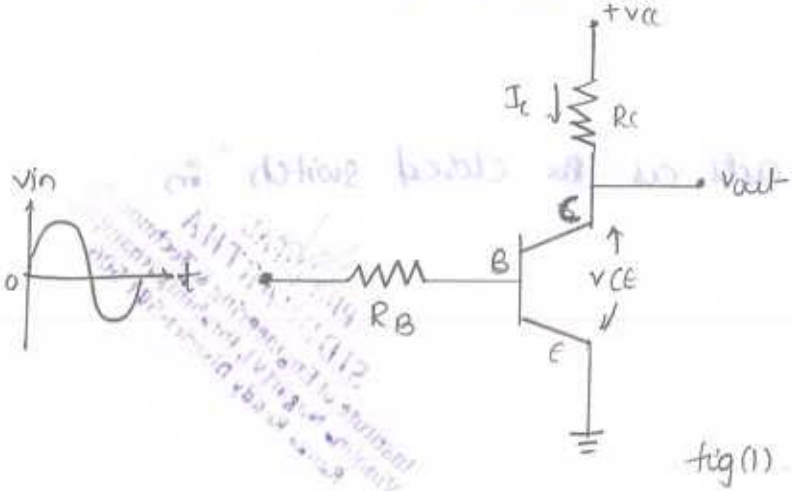
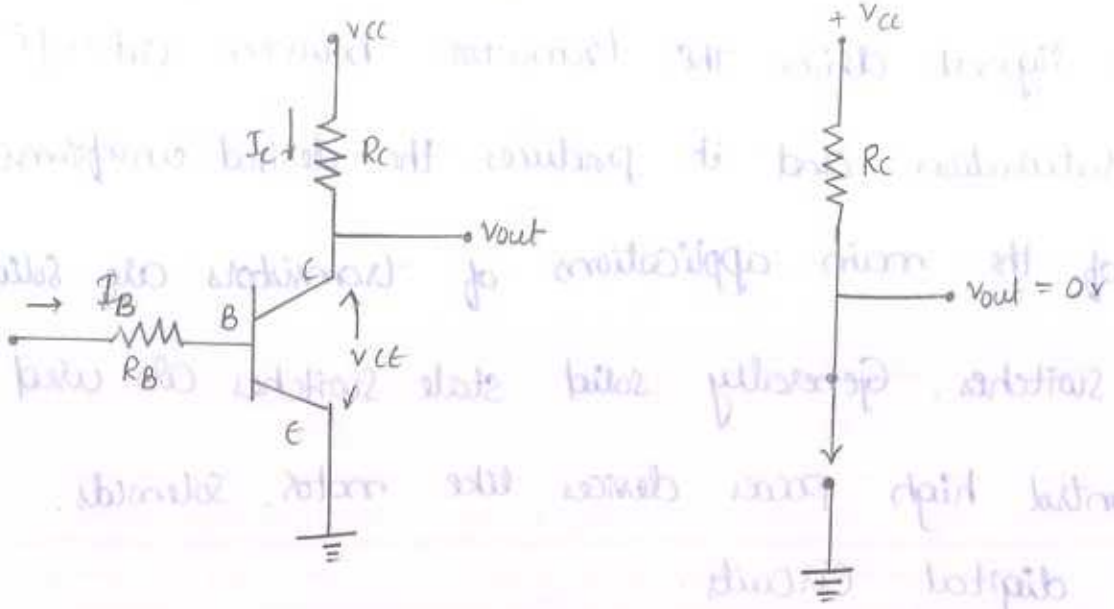


fig (1) Transistor CE Configuration

when the input applied to the CE configuration is high the base current I_B flows through circuit and it is as shown in fig(2)



fig(2) Transistor in saturation region (closed switch)

Apply KVL at the output side then,

$$V_{cc} = I_c R_c + V_{CE}$$

and I_B is very large when compared with I_c

Then

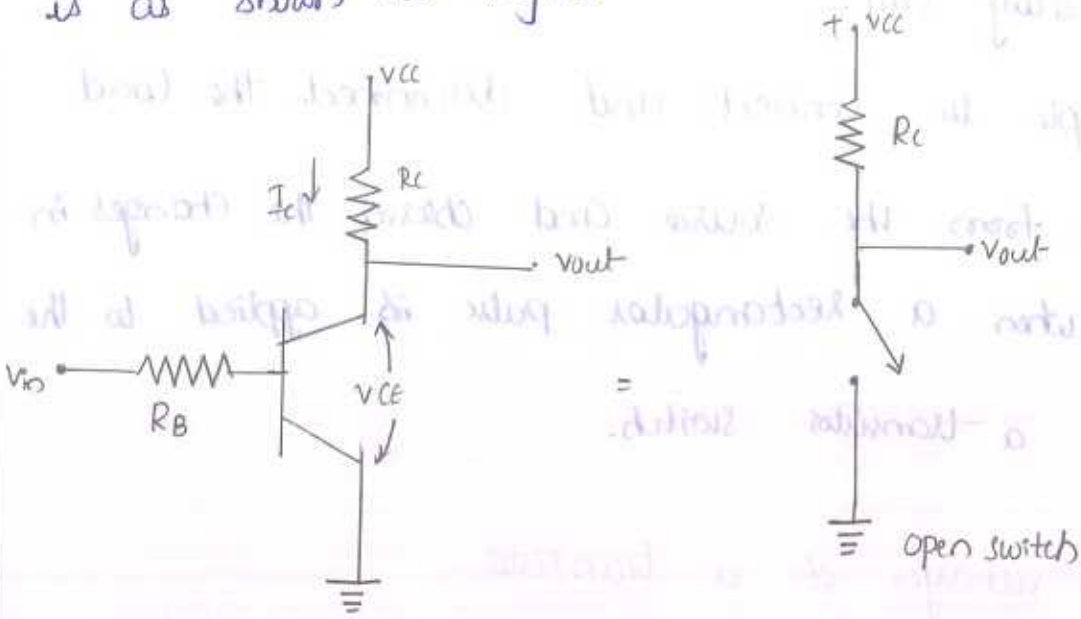
$$I_c = \beta I_B$$

$$\Rightarrow I_B >>> \frac{I_c}{\beta}.$$

Hence the transistor acts as the closed switch in

Saturation region

when input applied to the circuit is low. it means that there is no base current and circuit diagram is as shown in fig (3)



fig(3) Transistor in cut off region (open switch)

Apply KVL at the output side

$\Rightarrow V_{CC} = I_C R_C + V_{CE}$

But $I_B = 0 \Rightarrow I_C = \beta I_B$

$\Rightarrow I_C = 0$

Therefore $V_{CC} = 0 + V_{CE}$

$\therefore V_{CC} = V_{CE}$

Hence. in cut-off region the transistor acts as open switch.

Transistor as a switch can be used for connecting and disconnecting loads. switching light bulb, D.C motors, LED or relay coil.

for example to connect and disconnect the load resistor R_L from the source and observe the changes in output when a rectangular pulse is applied to the base of a transistor switch.

3.4 Breakdown voltages of a transistor

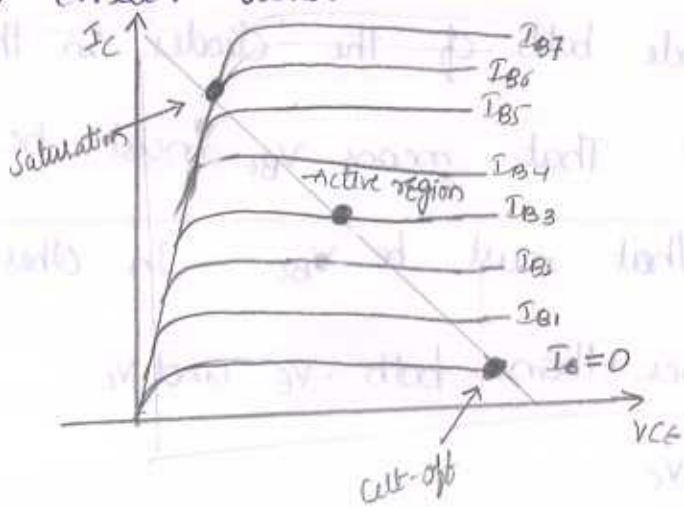
The reverse bias voltage beyond which the transistor may not function properly (or gets damaged) is known as breakdown voltage and the phenomena on is known as breakdown.

Breakdown in transistor is characterised by the application of a reverse bias voltage, across two of the three terminals with the third terminal left open-circuited.

* These breakdowns are of two types
1) Avalanche multiplication / avalanche breakdown
2) Reach-through or punch-through.

This breakdown voltage is a characteristic of the transistor alone. Breakdown occurs because of avalanche multiplication of the current I_{CO} that crosses the collector junction. As a result of this multiplication, the current is multiplied by a large factor M. We neglect leakage current, which does not flow through the junction and therefore is not subject to avalanche multiplication. At a high enough voltage, namely BV_{CBO}. The multiplication factor M becomes almost infinite. At this point the transistor attains breakdown. Here the current rises abruptly and large changes in current accompany small changes in applied voltage. The avalanche multiplication factor M depends on the voltage V_{CB} b/w collector & Base.

→ Common-Emitter transistor switch.



$I_B = \frac{I_C}{h_{FE}}$ (in active region)

$I_B > \frac{I_C}{h_{FE}}$ (in saturation)

Operating point in cut-off and saturation region.

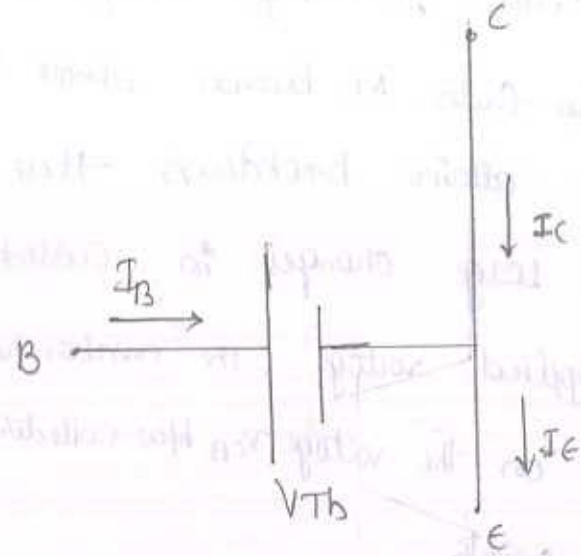
Load line Equation.

$V_{CE} = V_{CC} - I_C R_C$.

The point of intersection of this load line with the device characteristics is known as a operating point

Transistor in Saturation.

Saturation is the on mode of a transistor. A transistor in saturation mode acts like a short circuit between Collector and Emitter



In saturation mode both of the 'diodes' in the transistor are forward biased. That means V_{BE} must be greater than 0. and so that must be V_{BC}. In other words. V_B must be higher than both V_E and V_C

$$V_B > V_C$$

$$V_B > V_E$$

Because the junction from base to Emitter looks just like a diode in reality. V_{BE} must be greater than a threshold voltage to Enter Saturation.

The resistance r (also designated as R_f and called the forward resistance) takes on added physical significance even for this large signal model. model, where as static resistance $R = V/I$ is not constant and is not useful.

* Diode switching times.

The accumulation of charge in forward bias and depletion of charge in reverse bias do not allow the semiconductd diode to make abrupt ON-to-OFF and OFF-to-ON transitions.

Forward recovery time

The forward recovery time does not pose any limitation on switching speed of the diode in practice.

The forward recovery time denoted by t_{fr} of a semiconductd diode is negligible.

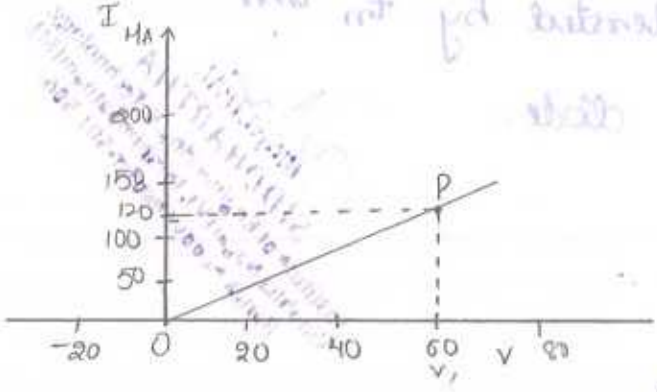
Reverse recovery time.

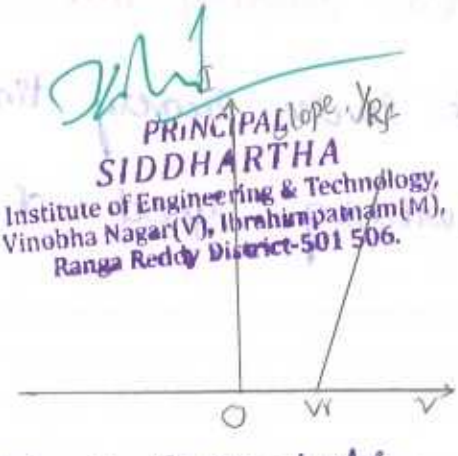
The reverse recovery time denoted by t_{rr} time limits the switching speed of the diode.

* Piecewise Linear Diode characteristics.

A large-Signal approximation which often leads to a Sufficiently accurate Engineering solution is the piecewise linear representation. This piecewise linear model replaces the diode by an open Circuit (infinite back resistance). if $v<0$ and a Constant forward resistance of $60/0.12 = 500\ \Omega$ for $v>0$. In this case, where the characteristic is a straight line passing through the origin, the dynamic resistance dv/dI Equals the static resistance v/I and the break-point or Cut-in voltage V_γ is Zero.

The piecewise linear approximation for a semiconductor diode characteristic is indicated in fig. The breakpoint is not at the origin and hence V_γ is also called the Offset or threshold voltage. The diode behaves like an open Circuit if $v<V_\gamma$ and has a Constant incremental resistance $r = dv/dI$ if $v>V_\gamma$.



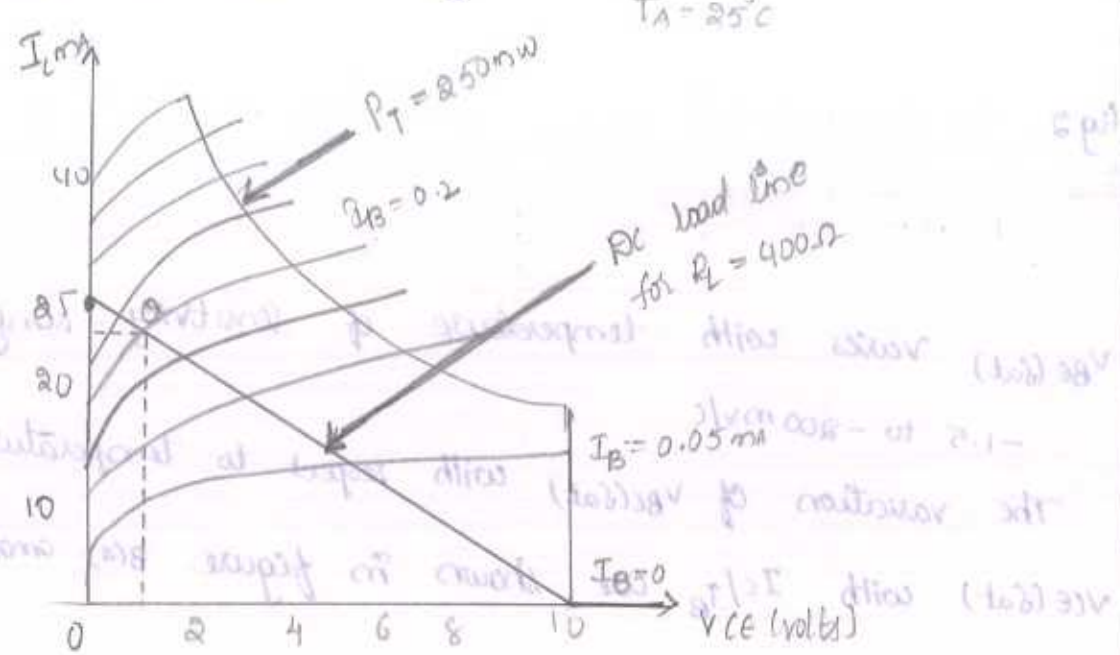


The piecewise linear characterization of a diode, a semiconductor.

3.6 Transistor in saturation

A transistor is said to be in saturation when the Emitter and collector diodes are forward biased

Consider the output characteristics of an n-p-n transistor in CE mode as shown in figure 1.



Typical characteristics of an n-p-n transistor in CE mode.

Since I_B is inversely proportional to I_C. at a point the saturation is reached where the collector current does not increase further irrespective of increasing base current. I_B is also inversely related to $V_{CE(sat)}$.

Hence, $V_{CE(sat)}$ and I_C depends on I_B.

Following figure (2) illustrates the variation of $V_{BE(sat)}$ as a function of I_C/I_B.

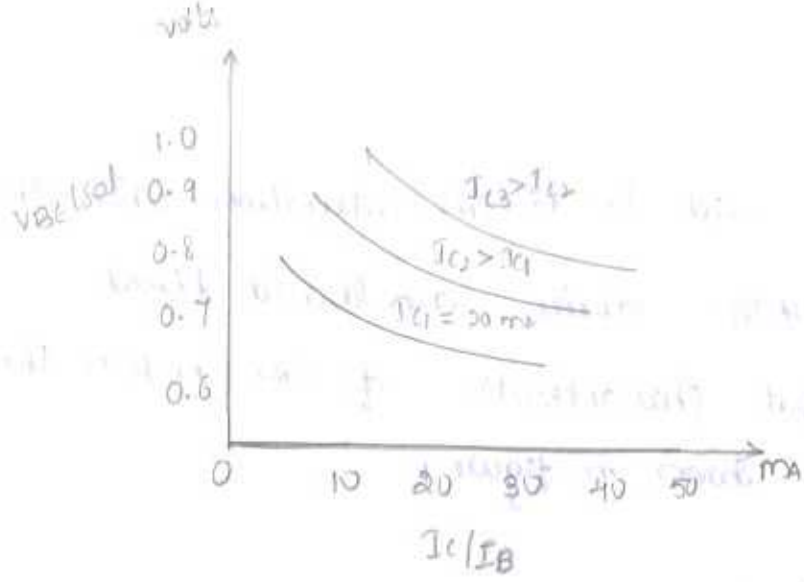
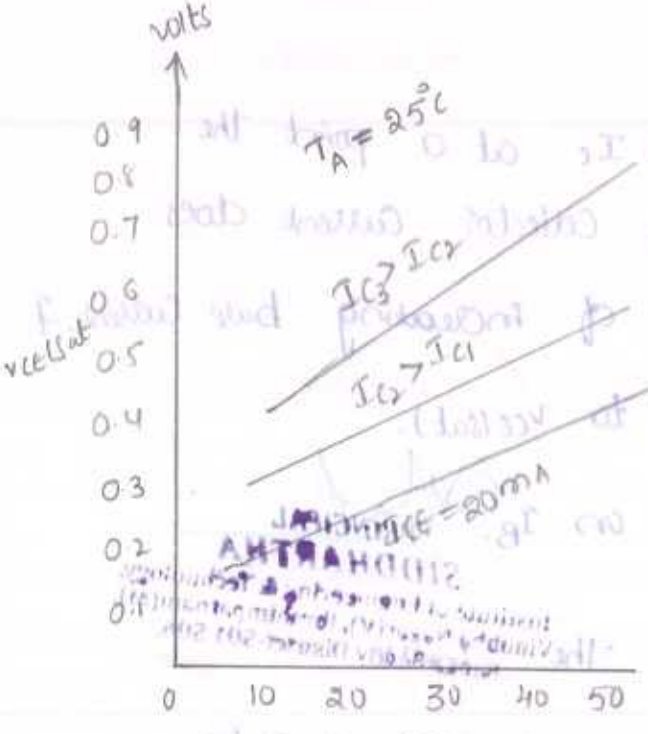


fig 2. The variation of $V_{BE(sat)}$ as a function of I_C/I_B with I_C as a parameter

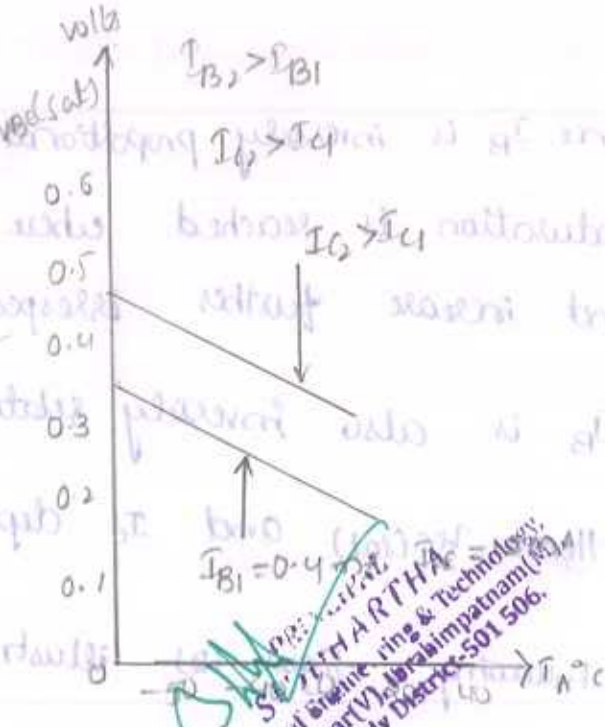
$V_{BE(sat)}$ varies with temperature of sensitivity range -1.5 to -200 mV/°C

-1.5 to -200 mV/°C

The variation of $V_{BE(sat)}$ with respect to temperature and $V_{CE(sat)}$ with I_C/I_B are shown in figure. 3(a) and 3(b)



a) The variation of $V_{CE(sat)}$ with of I_C/I_B for I_C as a parameter

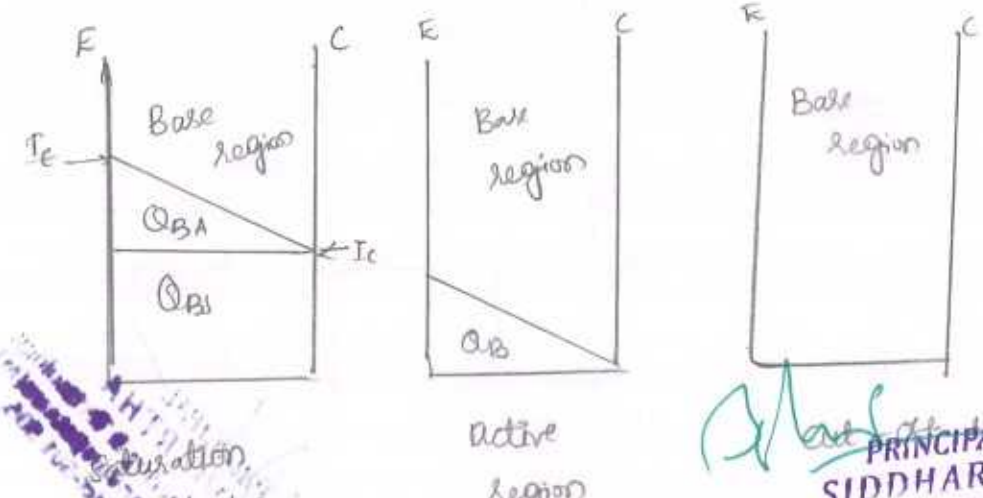


b) The variation of $V_{BE(sat)}$ as a function of temperature with I_B and I_C as a parameter.

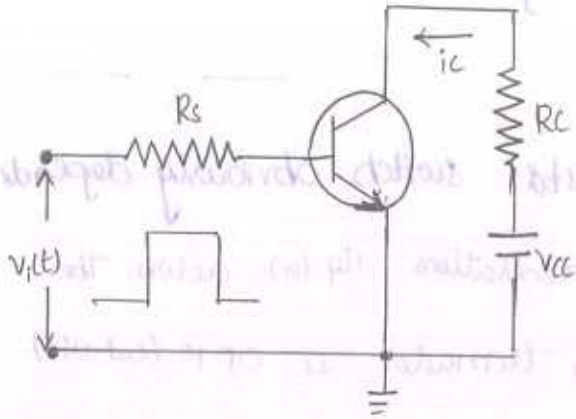
3.7 Switching Times in a transistor (or) Transistor Switching times.

The transistor is operated in saturation by forward biasing both Emitter junction and Collector – junction. In this case the Electron Concentrations within the P-type base region at the Emitter junction $x=0$ as well as the collector junction $x=w$ are determined by the forward bias voltage $+0.7V$.

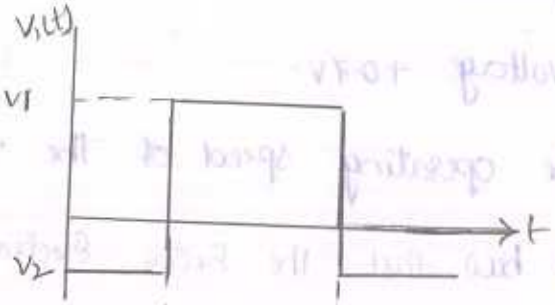
The operating speed of the transistor switch obviously depends on how fast the Excess Electron Concentrations fig (a) across the base region can change. When the transistor is OFF (cut-off) the P-type base region contains negligible Electron Concentration across it. on the other hand, the base region is fully saturated with Electrons when the transistor is ON Saturation



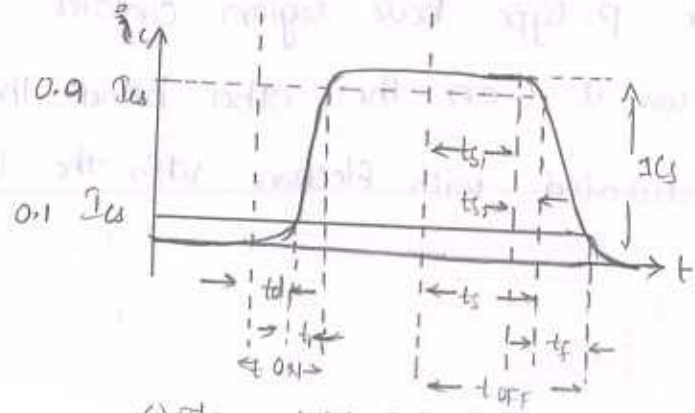
Let us Consider that the pulse input voltage $V_i(t)$ is applied across the Emitter-junction through the resistor R_s. There are two levels $-V_1$ and $+V_2$ in the input voltage waveform. The transistor has to change state when input makes positive and negative transitions between these two levels



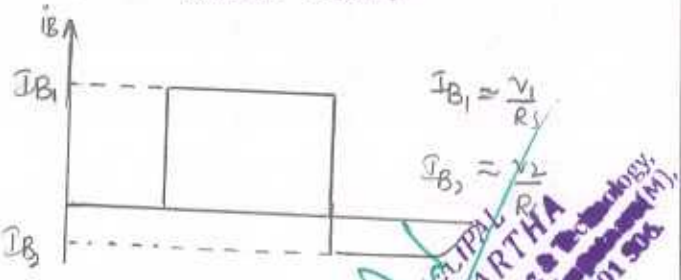
a) The pulse input voltage applied to Je through Rs



b) The input voltage pulse



c) The collector current



d) The base current

Transistor switching times

one at $t=0$ from $-V_1$ to $+V_2$ and the other at $t=T$ from $+V_2$ to $-V_1$.

A plot of the Collector Current i_c with Reference to the input $v_i(t)$ is indicated fig(b). The delay time t_d, Rise time t_r, Storage time t_s. and the fall time t_f are Graphically represented in the Collector Current waveform is shown fig (c)

3.8 Definitions of transistor Switching times

3.8.1 Delay time:

The delay time, t_d is the time required for the Collector current to change from zero (Cut-off) to 10 percent of the maximum current. approximately Equal to $I_{cs} \approx V_{cc}/R_c$. possible in saturation

3.8.2 Rise time.

The time required for the Collector current to rise from 10 to 90 percent of its saturation value I_{cs}. is defined as the rise time t_r. It is during the rise time the minority charge diffuses into the base from both Emitter and Collector

Turn ON time.

The sum of the delay time and rise time is defined as the turn-ON time, t_{ON}.

$$t_{ON} = t_d + t_r.$$

3.8.3 Storage time

The interval during which the base is depleted of Excess minority charge is defined as the storage time, t_s.

Graphically storage time is the interval during which the the Collector current drops from full to 90 percent of the saturation Current.

3.8.4 Fall time

The time required for the collector to drop from 90 to 10 per cent of the saturation Current is defined as the fall time, t_f.

3.8.5 Turn OFF time

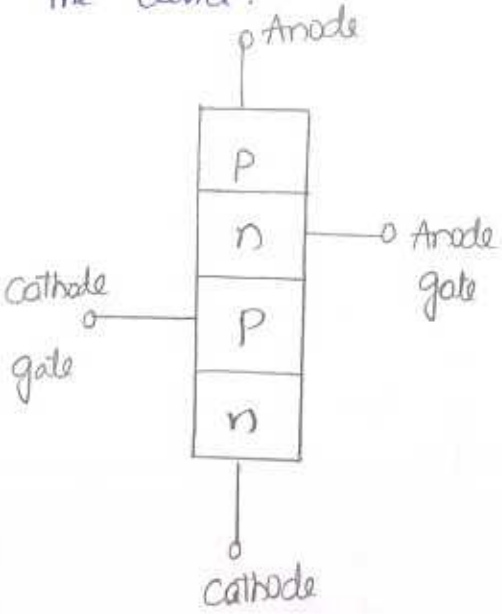
The sum of the storage time and the fall time is defined as the turn-OFF time t_{OFF}

$$t_{OFF} = t_s + t_f.$$

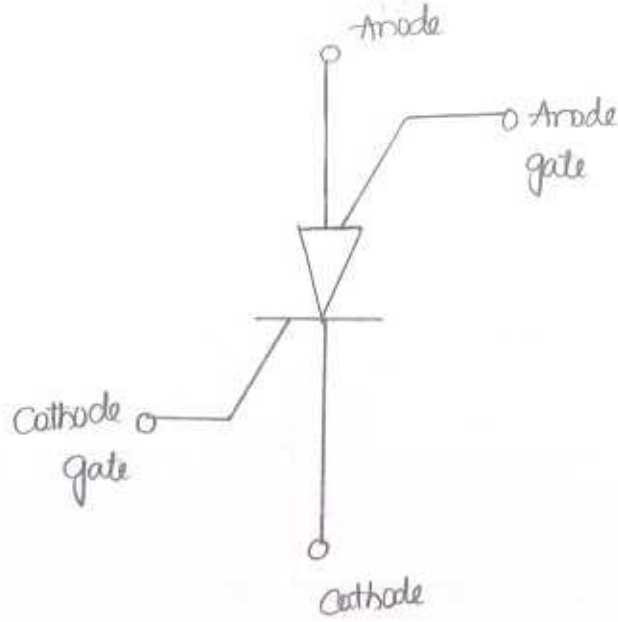
3.9 Silicon - Controlled Switch Circuits.

Silicon - Controlled switch Circuits are the four-layer diodes, in which p- and n- type layers are placed alternately as shown in figure 1(a). Sequence can be Either 'pnpn' or 'npnp'. These Circuits are also known as 'pnpn' and 'npnp' diodes or transistors.

Here anode current is used to turn-ON and turn-OFF the device.



a) Basic construction

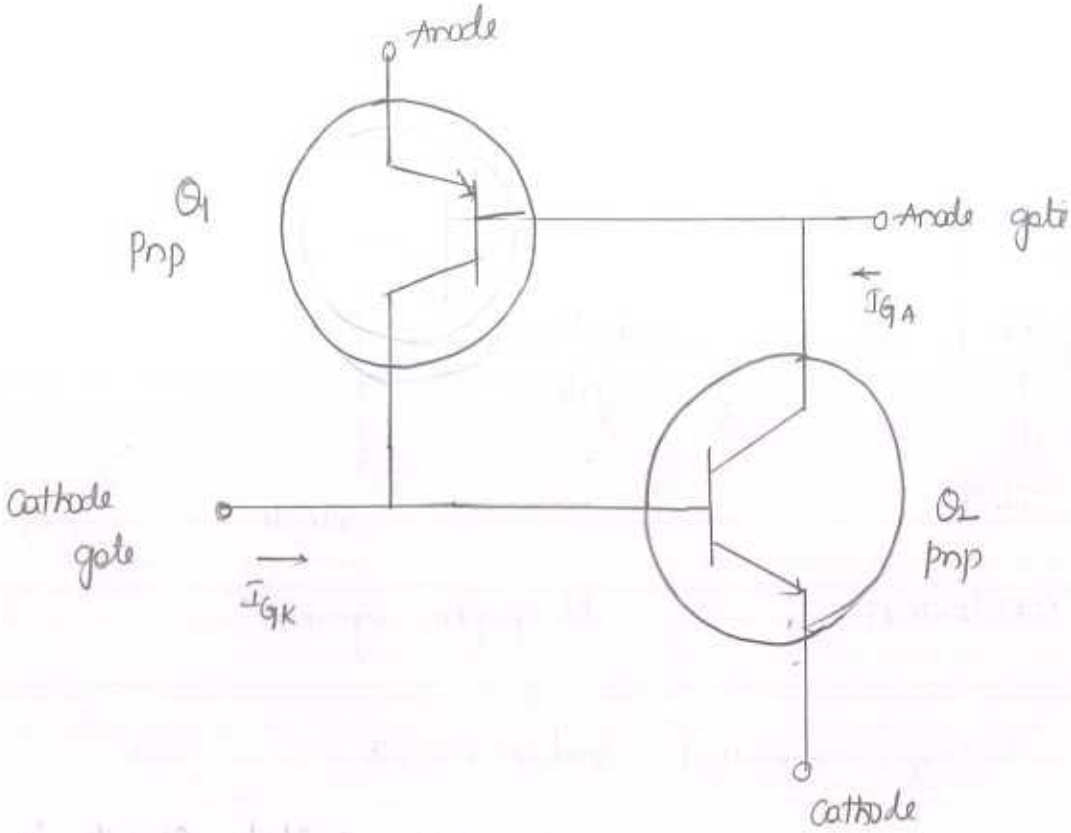


b) Graphic symbol

Silicon-Controlled Switch Circuits

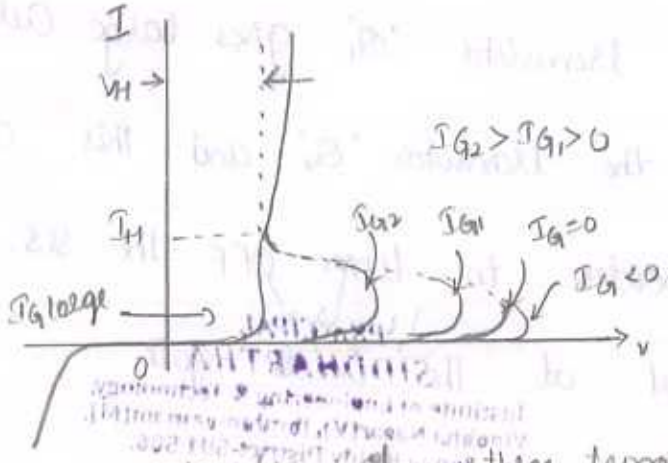
Equivalent silicon-controlled transistor switch circuit is shown below in figure (2). From the circuit, if the negative pulse is applied at the anode gate, transistor 'Q_1' gets forward-biased and will turn-ON. During ON-state transistor 'Q_1' gives large current I_{C_1} which turns-ON the transistor 'Q_2' and this action repeats, and inorder to turn OFF the SCS, a positive pulse is applied at the gate.

Generally the collector current I_{C_1} is larger than the cathode current which is required to turn-ON the transistor Q_2



Equivalent transistor circuit of Silicon Controlled Switch (SCS)

Characteristics of SCS.



Volt-ampere characteristic of three terminal SCS illustrating that forward breakover voltage is a function of the cathode-gate current

* UNIT- IV *

Multivibrators

→ Multivibrators are basically regenerative circuits comprising of two cross-coupled active devices like bipolar junction transistors. The Output states of a multivibrator depend upon the nature of coupling between the active elements involved.

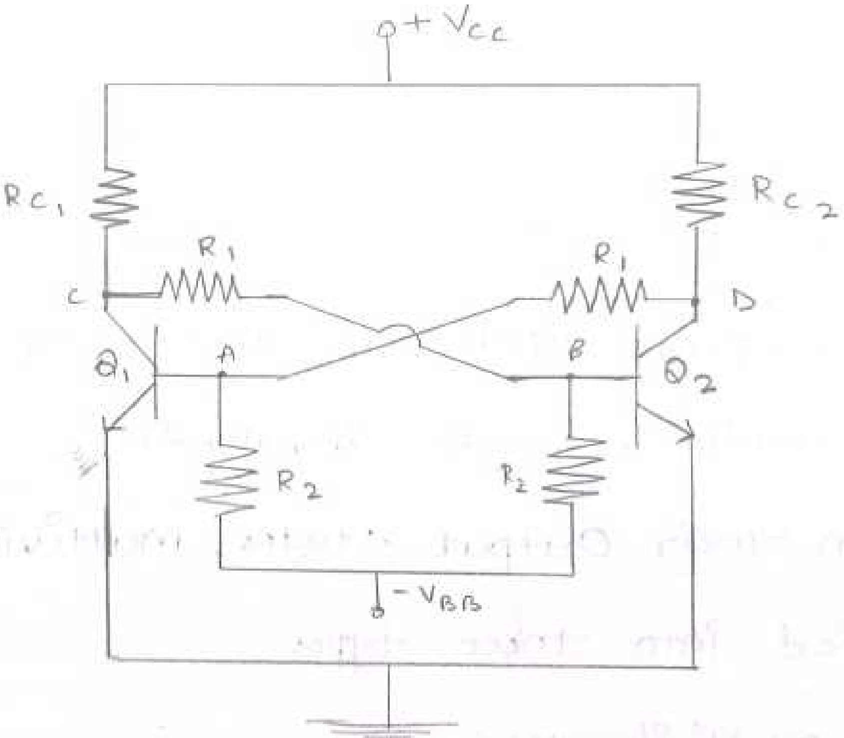
→ Based upon their Output states, multivibrators are classified into three types.

① Bistable multivibrators
② Monostable multivibrators and
③ Astable multivibrators.

1 Analysis and Design of Bistable Multivibrators:-

→ A bistable multi-vibrators has two stable Output states. It can remain indefinitely in any one of the two stable states and it can be induced to make an abrupt transition to the other stable state by means of suitable external excitation. It would remain indefinitely in this stable state, until it is again induced to switch into the original state by external triggering.

* Principle of operation of bistable multivibrator:-



→ Let us assume Q_1 and Q_2 to be n-p-n transistors. They are coupled to each other i.e; the collector current of Q_1 supplies the base-drive for Q_2; and the collector current of Q_2 provides the base-drive for Q_1.

→ When I_1 increases slightly, the voltage drop across the collector Resistance R_{c_1} increases. Since V_{cc} is fixed, the voltage of point C decreases. This has the effect of decreasing the base current of Q_2. This in turn, decreases the collector current of Q_2 viz I_2. If I_2 decreases, the voltage drop $I_2 R_{c_2}$ decreases. Hence the voltage of point 'D' increases. $[\because V_D = V_{cc} - I_2 R_{c_2}]$.

→ Due to increase of V_D the base current of Q_1 increases. This increases the collector current of Q_1 viz I_1. Thus I_1 further increases. $I_1 R_{C_1}$ drop further increases, V_c further decreases, the base current of Q_2 further decreases, with the result that I_2 further decreases.

→ Thus it can easily be seen that if the collector current I_1 increases even marginally, I_2 would go on progressively decreasing and as a result, I_1 would progressively increase. Eventually I_2 would become practically zero. At the same time transistor Q_1 would conduct heavily with the result that it would be driven into saturation. Thus Q_2 becomes 'OFF' and Q_1 becomes 'ON'.

→ It can similarly be shown that I_2 increases even marginally Similar sequence of operations would result and ultimately Q_2 would be ON, and Q_1 OFF.

→ Thus, when Q_1 is ON, Q_2 is Off and when Q_1 is OFF, Q_2 is ON. It may be noted that both transistors are not ON or OFF simultaneously.

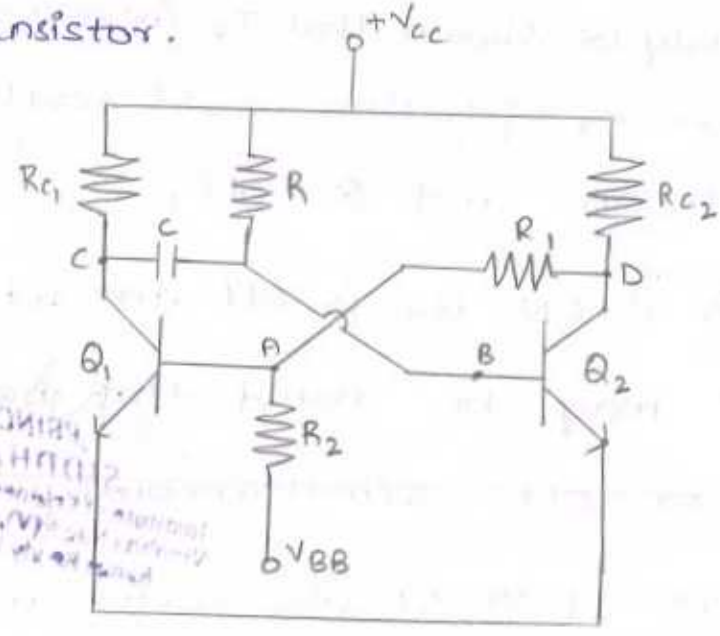
→ Thus there are two stable states which remain indefinitely.

2.2 Monostable Multivibrators :-

→ A monostable multivibrator has only one stable state, the other state being quasi-stable. Normally the multivibrator is in the stable state, and when an external triggering pulse is applied, it switches from the stable to the quasi-stable state. It remains in the quasi-stable state for a short duration, but automatically reverts i.e, switches back to its original stable state, without any triggering pulse.

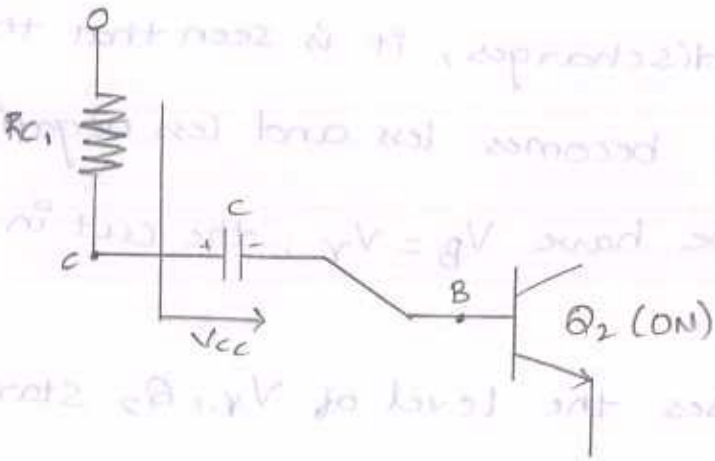
2.3 Principle of operation :-

→ A collector-coupled monostable multivibrator of the two transistors Q_1 and Q_2. Q_1 is normally OFF and Q_2 is normally ON. Resistors R_1 and R_2 are connected to normally OFF transistor, and the capacitor C is connected to the normally ON transistor.



→ It is seen from the circuit of the monostable multi that, under normal conditions, the supply voltage Vcc provides enough base drive to the transistor Q_2 through resistance R, with the result that Q_2 goes into saturation. with Q_2 ON, Q_1 goes OFF, as already studied in the context of binary operation.

→ with Q_2 ON and Q_1 OFF, the capacitor finds a charging path as shown in fig.

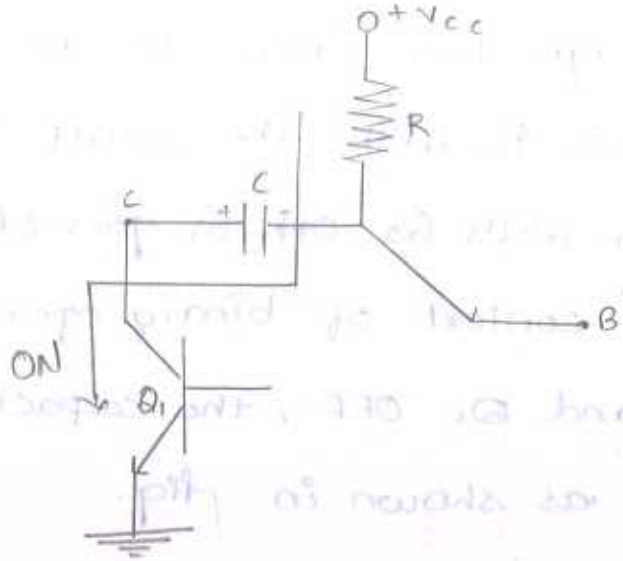


→ The voltage across the capacitor is Vcc with polarity as shown [Positive on the left, negative on the right].

→ It is obvious that in the stable state of the multi, Q_2 is ON and Q_1 is OFF.

→ If a negative triggering pulse is applied to the collector of Q_1, it is transmitted to the base of Q_2 through the capacitor, and hence makes it negative. Immediately Q_2 goes OFF & Q_1 becomes ON.

→ with Q_1 ON and Q_2 OFF, the capacitor C finds a discharging path as shown below fig.



→ As the capacitor discharges, it is seen that the potential of point B becomes less and less negative, and after a time, we have $V_B = V_\gamma$; the cut in voltage of Q_2.

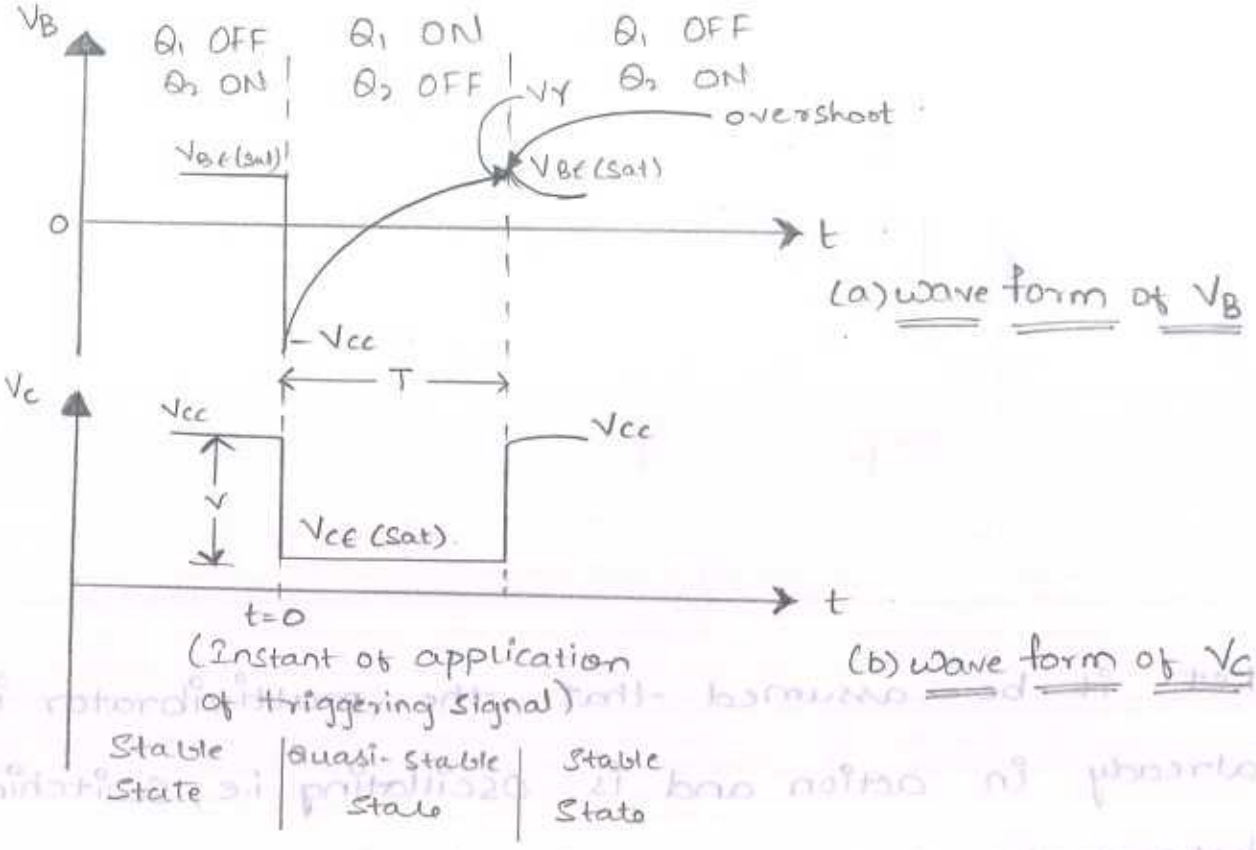
→ As soon as V_B crosses the level of V_γ, Q_2 starts conducting and gets saturated. when Q_2 becomes ON, Q_1 becomes OFF. Thus the original stable state of the multi is restored.

[In quasi-stable state : Q_1 is ON and Q_2 is OFF]

The interval during which the quasi-stable state of the multi persists i.e, Q_2 remains OFF is dependent upon the rate at which the capacitor C charges. This duration of the quasi-stable state termed as delay time or pulse width or gate time.

It is denoted as T.

→ The wave forms of the voltages at points B (Base of Q_2) and C (collector of Q_1) are as shown.



(a) wave form of V_B

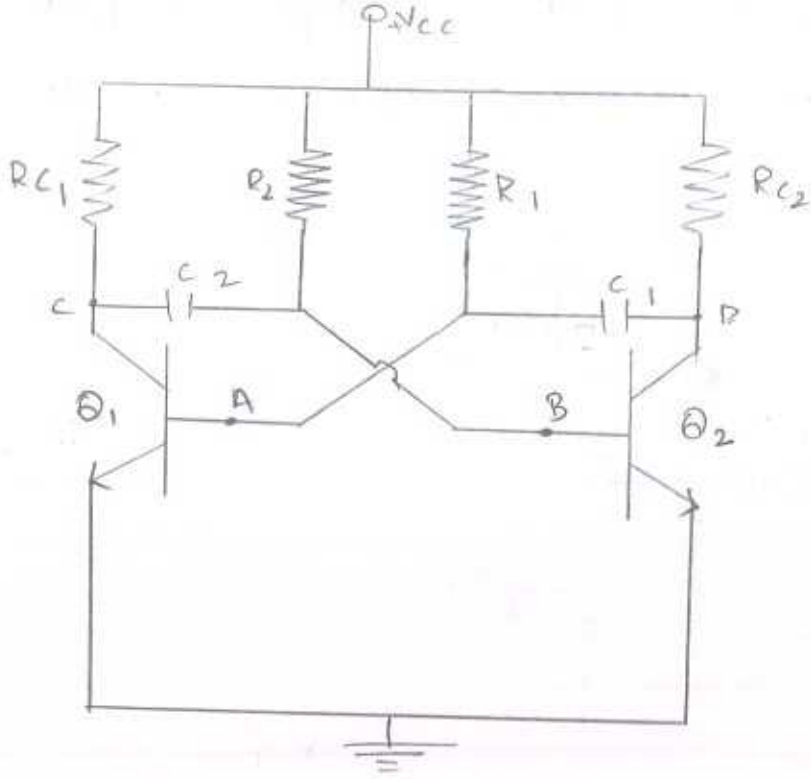
(b) wave form of V_C

1.3 Astable Multivibrators :-

→ An astable multivibrator has two quasi-stable states, and it keeps on switching between these two states, by itself. No external triggering signal is needed. The astable multi cannot remain indefinitely in any of these two states.

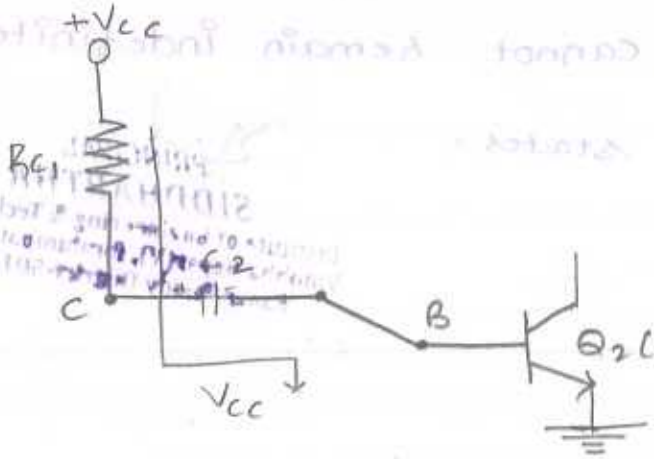
PRINCIPAL
SIDDHARTHA
Institute of Engineering & Technology,
Vinobha Nagar(V), Ibrahimpatnam(M),
Ranga Reddy District-501 506.

3.1 Principle of operation:-

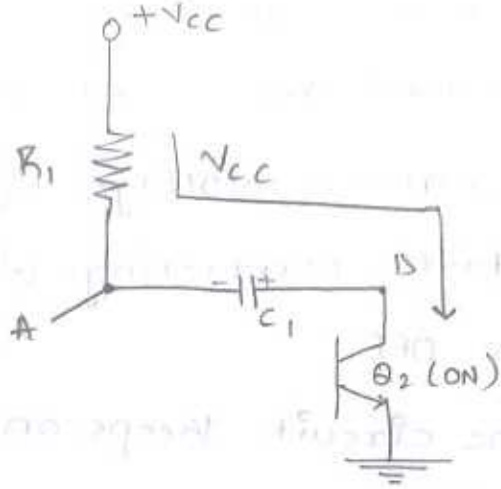


→ Let it be assumed that the multivibrator is already in action and is oscillating i.e, switching between the two states. Let it be further assumed that at the instant considered, Q_2 is ON and Q_1 is OFF,

(i) Since Q_2 is ON, capacitor C_2 charges through resistor R_{C_1} as shown



(ii) Capacitor C_1 discharges through resistor R_1, as shown

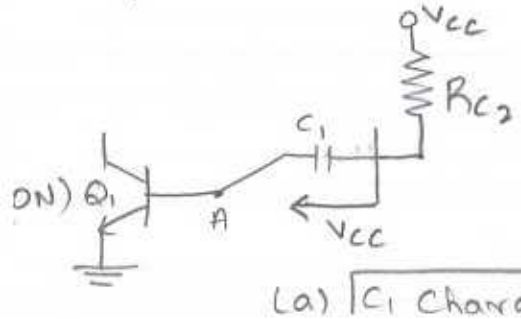


→ The voltage across C_1 when it is about to start discharging is V_{cc} with polarity.

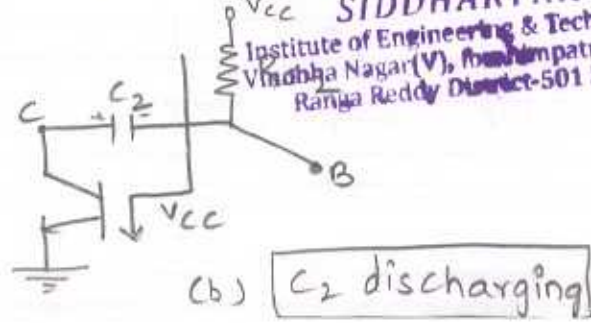
→ As capacitor C_1 discharges more and more, the potential of point A becomes more and more positive and eventually V_A becomes equal to V_γ, the cut in voltage of Q_1. For $V_A > V_\gamma$, transistor Q_1 starts conducting. When Q_1 is ON, Q_2 becomes OFF.

→ Similar operations repeat when Q_1 becomes ON and Q_2 becomes OFF.

→ Thus with Q_1 ON and Q_2 OFF, capacitor C_1 charges through resistor R_{C_2} and capacitor C_2 discharges through resistor R_2. The charging and discharging paths are as shown in below Fig (a) & (b).



(a) C_1 Charging

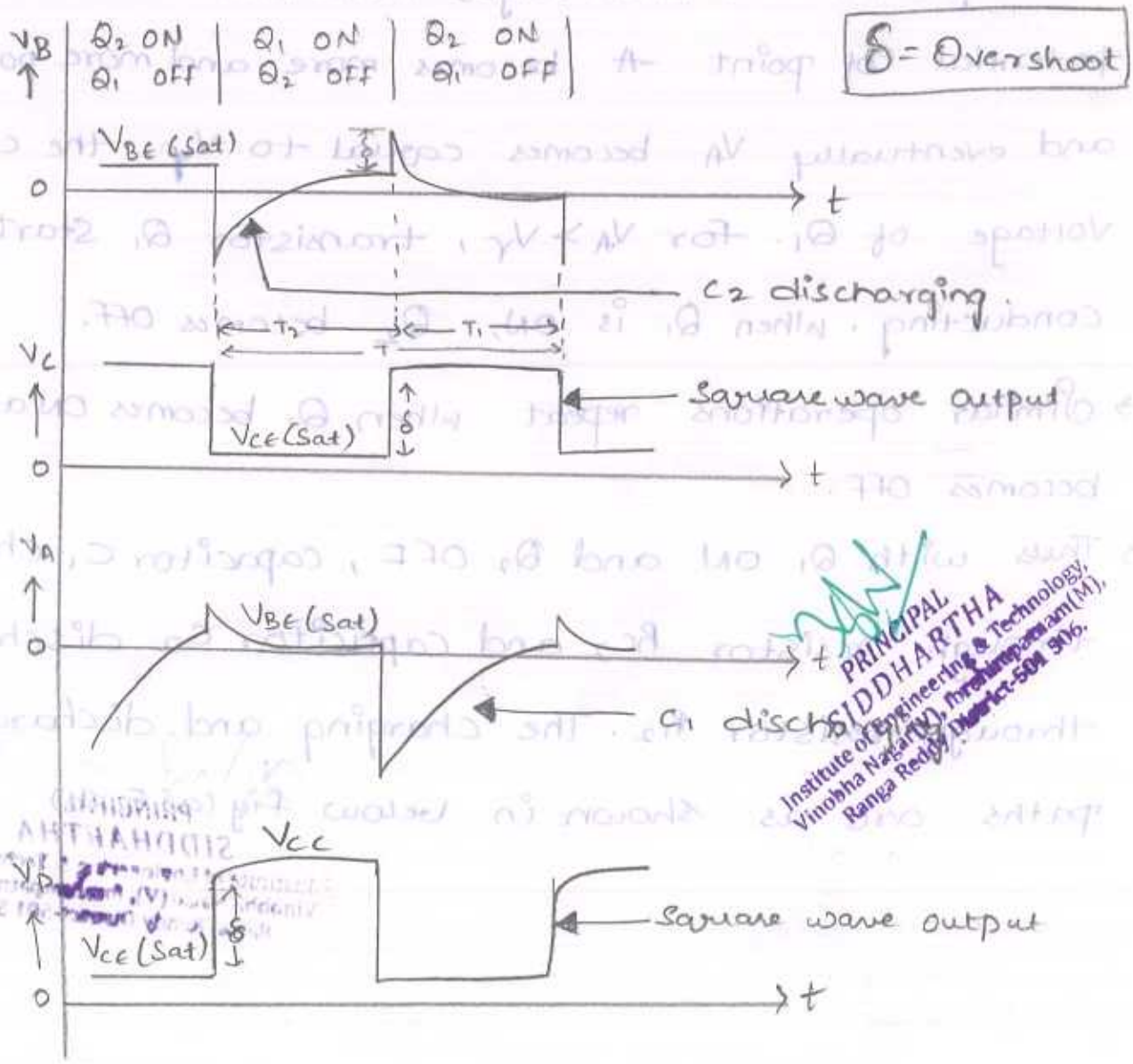


(b) C_2 discharging

→ As capacitor C_2 discharges more and more, it is seen that the potential of point B become less and less negative (or more & more positive), and eventually V_B becomes equal to V_γ, the cut-in voltage of Q_2. When $V_B > V_\gamma$, transistor Q_2 starts conducting. When Q_2 becomes ON, Q_1 becomes OFF.

→ It is thus seen that the circuit keeps on switching continuously between the two quasi-stable states and once in operation, no triggering is needed.

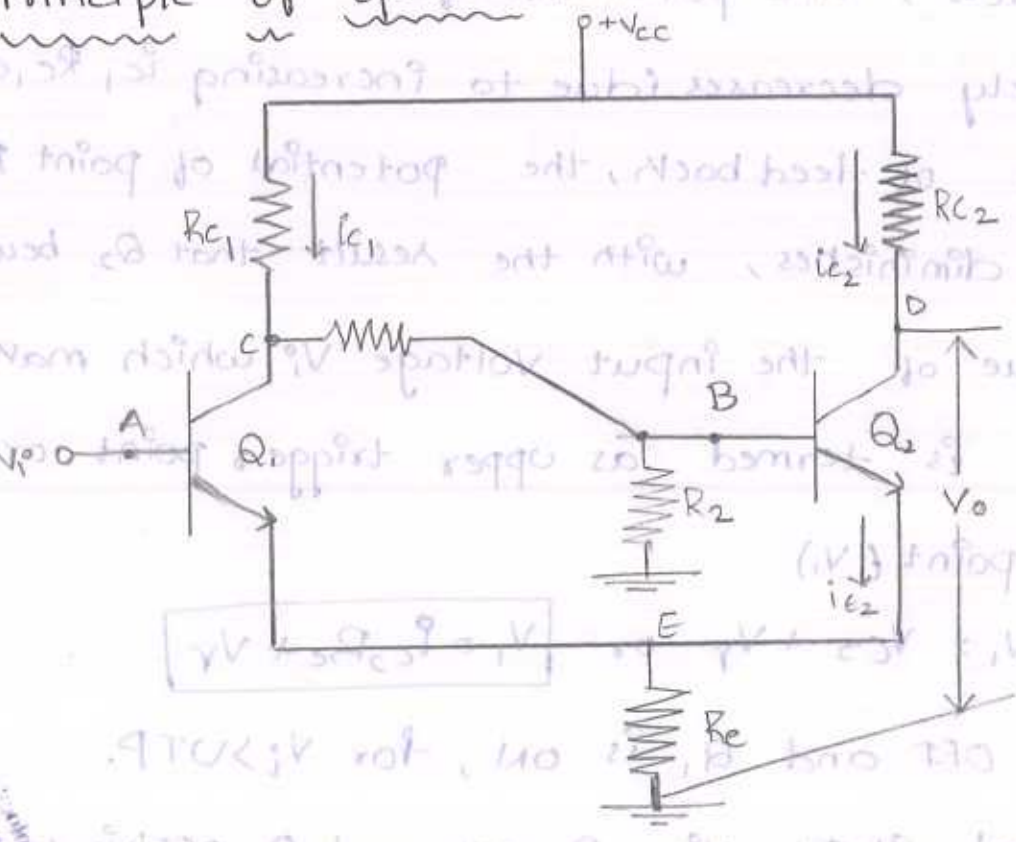
→ The Input & Output waveforms are shown.



4.4 Schmitt Trigger :-

→ Schmitt trigger is a special type of bistable multivibrator which is different from the basic binary circuit in that the resistive coupling between the Output of Q_2 and the Q_1 of the basic circuit is missing, although the collector of Q_1 and the base of Q_2 are coupled in usual manner.

4.4.1 Principle of operation :-



→ Let the input to the transistor Q_1 be a Sinusoidal voltage: $V_i = V_m \sin \omega t$

→ When $V_i = 0$, Q_1 is OFF. However Q_2 gets adequate base drive from the supply voltage V_{cc} and

hence it conducts, but it would be conducting in the active region.

→ Due to the flow of current i_{E_2} through R_e, there is a voltage drop $i_{E_2} R_e$.

Assuming $i_{E_2} = i_{C_2}$, we have $V_e = i_{C_2} \cdot R_e$.

From the ckt, it is evident that for Q_1 to conduct, V_i should rise to the voltage $(V_\gamma + V_\gamma)$, where V_γ is the cut in voltage of Q_1

→ As Q_1 conducts, the potential of it's collector terminal C progressively decreases (due to increasing $i_{C_1} R_{C_1}$ drop), and because of feed back, the potential of point B progressively diminishes, with the result that Q_2 becomes OFF. This value of the input voltage V_i which makes Q_1 conduct is termed as upper trigger point or (UTP) upper trip point (V_1)

$$\therefore V_1 = V_{E_2} + V_\gamma \text{ or } \boxed{V_1 = i_{C_2} R_e + V_\gamma}$$

→ Now Q_2 is OFF and Q_1 is ON, for $V_i > UTP$.

→ If the original state viz Q_2 ON and Q_1 OFF is to be restored, it is essential that V_1 decreases.

→ As V_1 decreases, i_{C_1} decreases volt drop $i_{C_1} R_{C_1}$ decreases and hence potential of point B and hence that to B would increase.

and eventually when V_B becomes equal to $V_A = V_{BE(act)} + V_E$; Q_2 starts conducting, and Q_1 goes OFF.

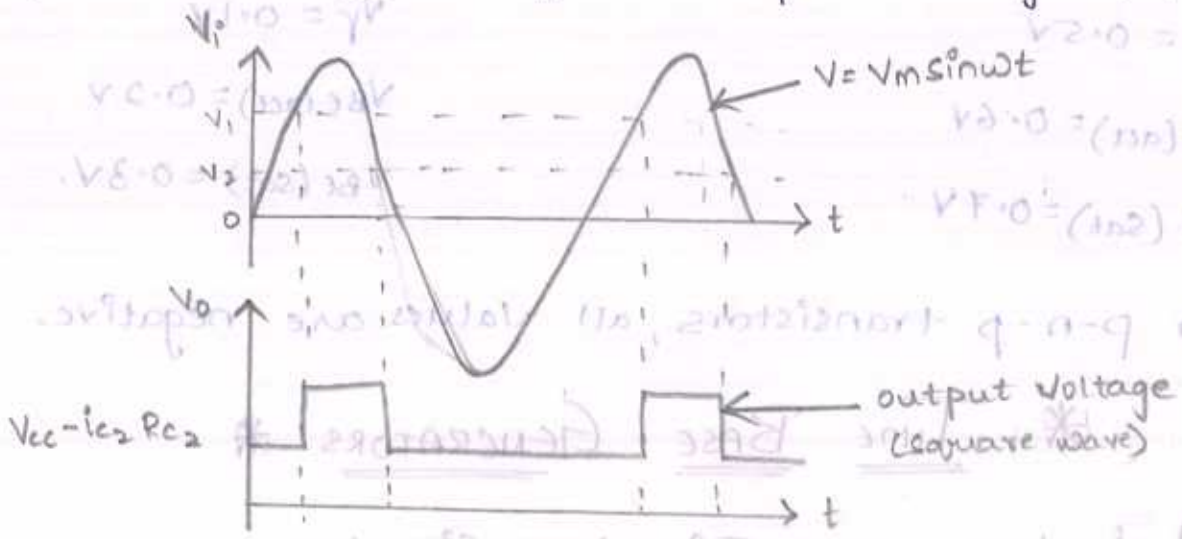
This value of the input voltage which makes Q_2 conduct again is termed as lower trigger point (LTP)(V_2)

$\therefore V_2 = V_{BE(act)} + V_E$ or $\boxed{V_2 = V_{BE(act)} + I_{C_1} R_e}$

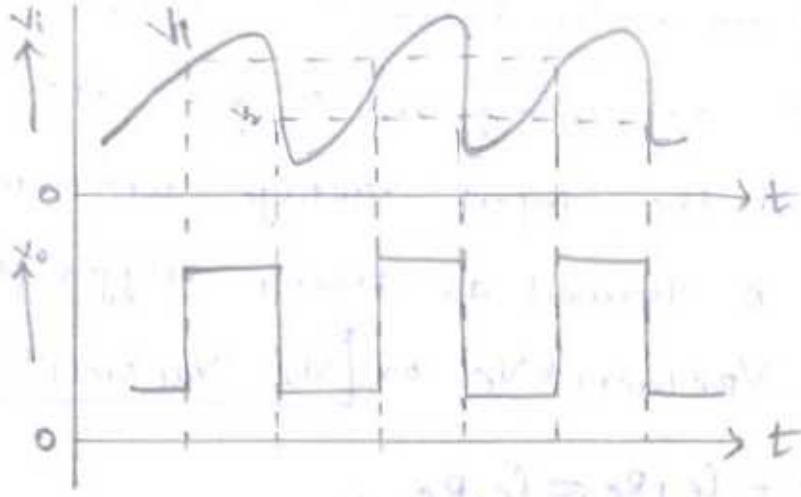
$\because V_E = I_{E_1} R_e \approx I_{C_1} R_e$.

→ $\boxed{\begin{aligned} UTP &= V_1 + V_\gamma + I_{C_2} R_e; \text{ and} \\ LTP &= V_2 = V_{BE(act)} + I_{C_1} R_e \end{aligned}}$

→ UTP, LTP are values of the input voltage V_i.



→ It is observed that the Output is an unsymmetrical square wave. Thus the Schmitt trigger readily converts sinusoidal wave to square wave. Hence, it termed as sine to square converter or squaring circuit. The Output of a schmitt trigger is a square wave, whatever the wave form of input signal.



The following values may be assumed for n-p-n silicon and germanium transistors.

(i) Silicon transistor.

$V_\gamma = 0.5V$

$V_{BE(act)} = 0.6V$

$V_{BE(sat)} = 0.7V$

(ii) Germanium transistor.

$V_\gamma = 0.1V$

$V_{BE(act)} = 0.2V$

$V_{BE(sat)} = 0.3V.$

→ for p-n-p transistors, all values are negative.

*4.2 Time Base Generators *

2. General features of a Time base signal:-

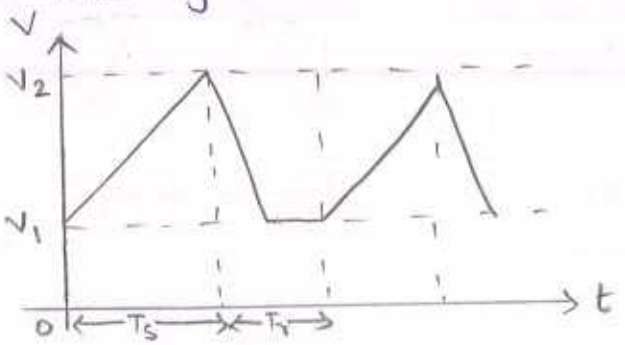
→ A time-base generator is an electronic circuit which generates an output voltage or current that varies linearly with time. Ideally, the waveform of the output should be a ramp. The foremost application of such a ramp voltage is in a cathode ray oscilloscope, for deflecting the electron

beam horizontally across the screen. Since the applied voltage makes the electron beam sweep across the screen, it is termed as sweep voltage, and the circuit generating the sweep voltage is termed as sweep generator. In practice, there are both kinds of sweep generators : Voltage sweep generators and current sweep generators.

Time base generators find use not only in CRO's, but in many other application areas also, like radar, television, time modulation, precise time measurements etc.

2.2 General wave form of time-base (or sweep) voltage :-

→ A sweep voltage which, ideally, varies linearly with time has the general wave form.



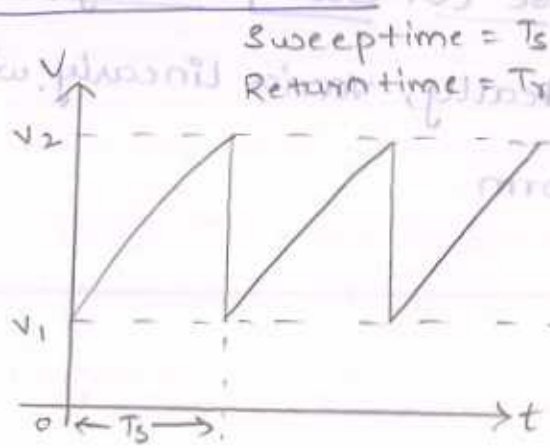
T_s --- Sweep time

T_r --- Return time.

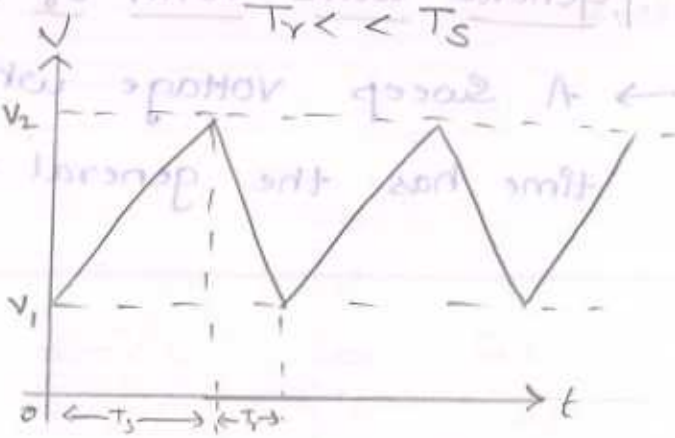
→ From the figure, it is evident that the voltage, starting from an initial value, V_1 rises linearly to a peak value V_2, and falls to the initial value V_1 over a short period of time. The time taken by the wave to reach the maximum value, starting from the initial value, is termed as sweep time, and the

time during which it returns to the initial value is termed as <u>return time</u> or <u>restoration time</u> or <u>fly-back time</u>. Sweep time is denoted as T_s and return time is denoted as T_r.

The return time T_r and the wave shape during the return time normally do not matter. But in some special applications, the restoration time T_r should be quite small in comparison with the sweep time T_s. If the voltage returns to the initial value instantaneously, the wave form would be shown in fig. It is termed as <u>Saw-tooth wave</u>.



Saw tooth wave



Triangular wave

4.8.2 Methods of Generating time-base waveform:-

→ There are many practical methods by which Sweep voltages, which are practically linear can be generated. The most important amongst these are as follows

① Exponential charging:-

→ In this method, a capacitor is charged through a resistor to a voltage which is quite small as compared to the charging voltage.

② Constant current charging:-

→ In this method, a capacitor is charged from a constant current source. As will be seen later, the voltage across the capacitor is a ramp voltage.

③ Miller circuit:-

→ In this, a step voltage is converted into a ramp, using an integrating circuit like the miller integrator.

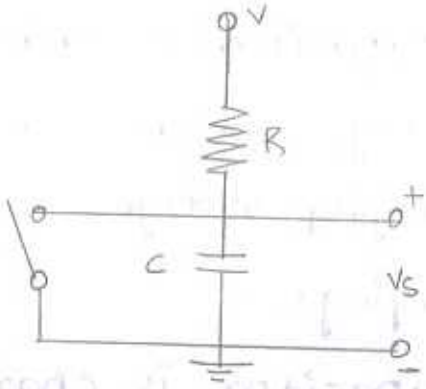
④ Boot strap circuit:-

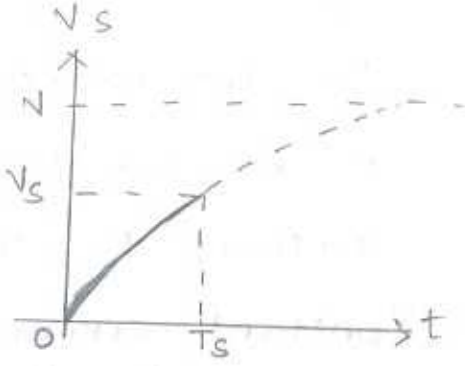
→ In this method, a constant current is passed through a capacitor and the voltage across the capacitor is a ramp. Constant current is obtained by maintaining a constant voltage across a fixed resistor in series with the capacitor.

⑤ Compensating Networks:-

→ To improve the linearity of Boot strap time-base generators, several compensating circuits are introduced.

2.2 Exponential Sweep circuit :-





General wave

→ S is a switch which can open or close. Let it be assumed that S opens at $t=0$. An exponential output is given as $\boxed{V_s = V(1 - e^{-t/RC})}$

→ When the sweep amplitude has attained the value V_s, Let it be assumed that switch S closes. The wave form of the sweep voltage generated is shaon by the thick Line. Let $V_s = V_s$ at $t = T_s$. The sweep error of the above wave is $e_s = \frac{V_s}{V}$.

→ It is evident that as the ratio $\left[\frac{V_s}{V}\right]$ decreases, Hence the linearity of the wave improves.

→ It has also been studied earlier, $T_s << RC$.

$$e_s = \frac{T_s}{RC}$$

Putting $RC = \tau$, the time constant of the circuit we have

Slope $\boxed{e_s = \frac{T_s}{\tau}}$

→ For linearity of a wave form, e_s should be as small as practiable. Hence τ must be quite large in comparison with T_s.

We have also proved that for the exponential wave in question, transmission error $e_t = \frac{T_s}{2RC}$.

(or) $\boxed{e_t = \frac{1}{2} \cdot \frac{T_s}{\tau}}$, and

displacement error $e_d = \frac{T_s}{BRC}$ or $\boxed{e_d = \frac{1}{8} \cdot \frac{T_s}{\tau}}$.

Note:- Let a capacitor C be charged with constant current I

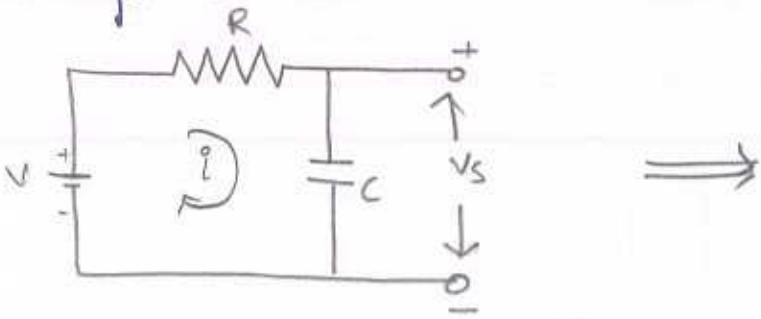
The voltage across, $C = \frac{Q}{C} = \frac{It}{C}$.

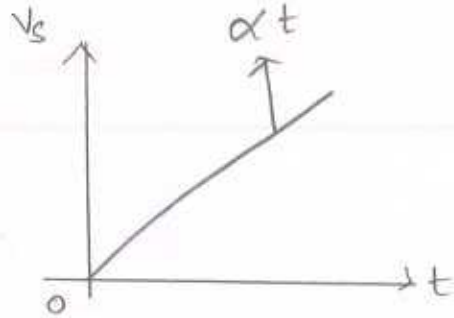
$\therefore$ Rate of change of voltage with time $= \frac{(It/C)}{t}$

Hence $\boxed{\text{Sweep speed} = \frac{I}{C}}$.

2.3 Boot Strap Sweep Generator:-

→ The basic principle involved in Generating a ramp voltage is as





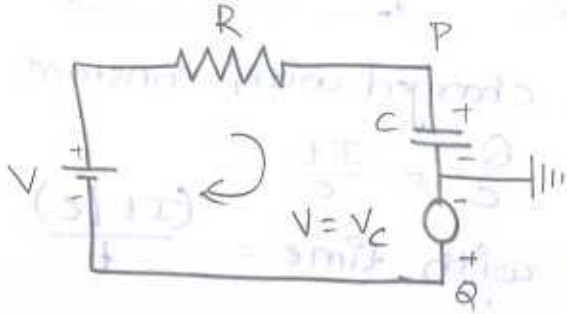
→ we have $V_s = \frac{1}{C}\int i\,dt$.

→ capacitor acts as short-circuit when $t = 0$, and as open circuit when steady state has been reached.

$V_s = \left[\frac{I}{C}\right]t$.

Let $\frac{I}{C} = \alpha$ $\therefore$ $\boxed{V_s = \alpha t}$ → Ramp voltage.

→ The capacitor current can be maintained constant by incorporating an auxiliary voltage source such that the source voltage is always equal to the capacitor voltage but acts in opposition to it.



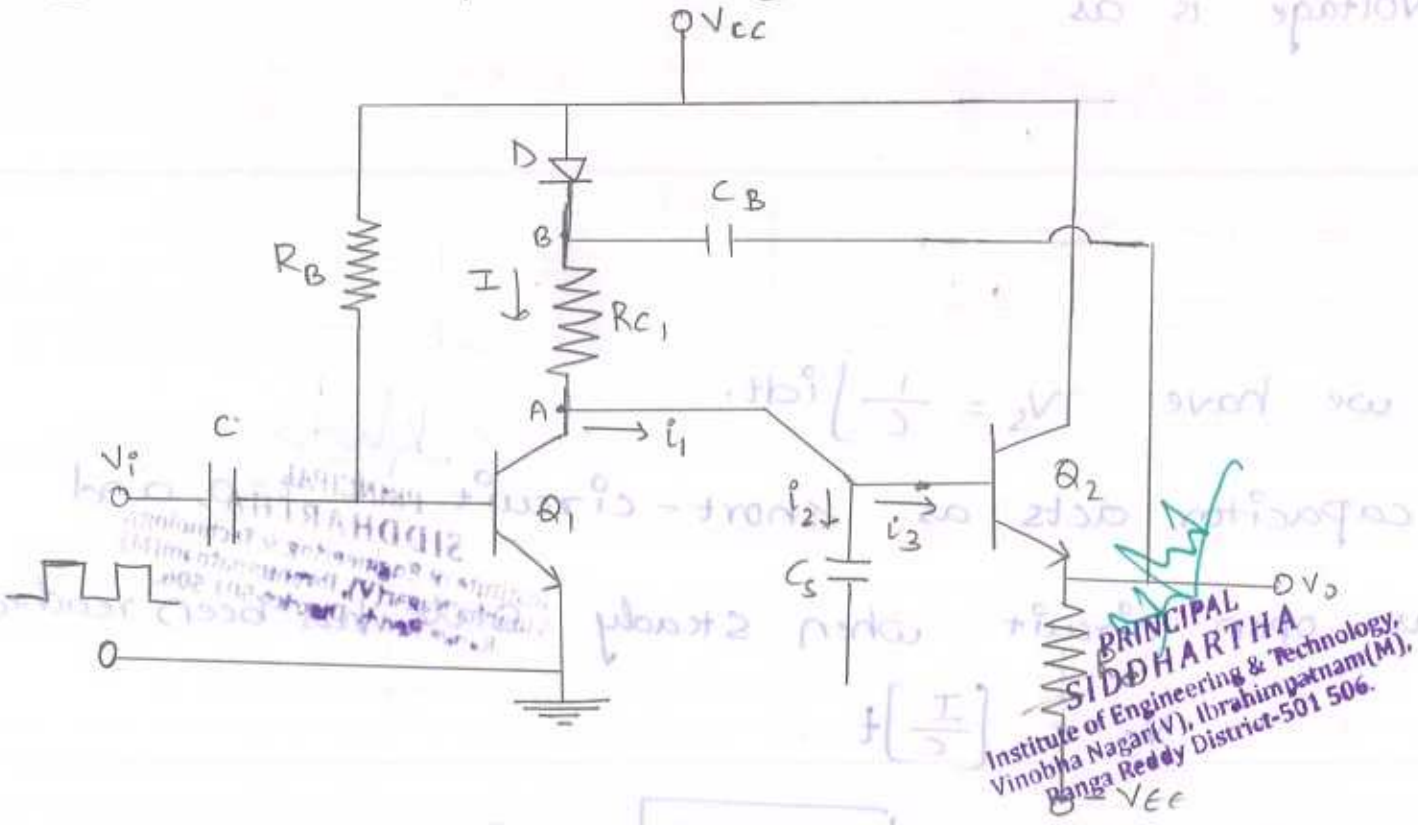
If $V = V_c$ in magnitude but opposite in direction, so the net voltage across PQ = 0

$\therefore$ current $I = \frac{V}{R}$

→ Since both V and R are of fixed magnitude current I is constant." This constant current I flowing through capacitor develops a ramp voltage across it."

4.2.3 Transistor Bootstrap Time Base Generator

(Bootstrap Sweep circuit :-)



Switch ← | → Emitter follower

→ The bootstrap Sweep circuit use the principle of Bootstrap Sweep Generator & Generates a ramp voltage.

→ The transistor Q_1 acts as ON-OFF Switch, and the transistor Q_2 is an emitter-follower.

→ The input V_i is a pluse voltage, or Rectangular wave.

→ When the input Signal V_i is positive, transistor Q_1 becomes ON i.e, goes into Saturation.

∴ potential of 'A' point; $\boxed{V_A = V_{CE(Sat)}}$.

→ Q_2 is coupled to collector of Q_1. Hence point B becomes negative w.r.t V_{cc}, Diode D readily conducts. ∴ $\boxed{V_B \approx V_{cc}}$

→ When the input V_i goes negative, Q_1 becomes OFF. The potential of 'A' Rises. This voltage increase at A is transmitted to B through Q_2 & capacitor C_B. The result is potential of B also rises by Same amount.

→ This is principle of boot strap. Thus V_B rises from V_{cc} to $(V_{cc} + V_A)$.

→ we have $I = \frac{V_B - V_A}{RC_1} = \frac{V_{cc}}{RC_1}$ $\left[\because V_B = V_{cc} + V_A\right]$.

→ Since both V_{cc} & RC_1 are fixed, V_{cc} is constant. Hence current I is constant in magnitude.

→ Since Q_1 is cut off collector current is zero. $I = i_1$

But $i_1 = i_2 + i_3$. Since Q_2 is an emitter follower,

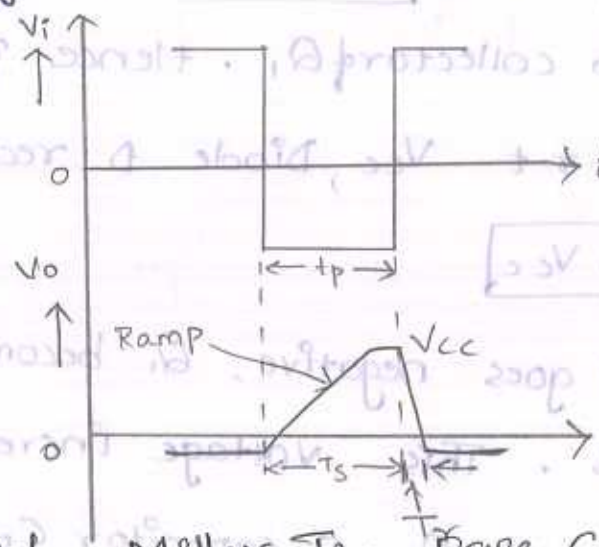
its input impedance is very very high $i_3 = 3\alpha$..

$\therefore i_1 = i_2 = I$.

→ As this current flows through 'C_s' a ramp voltage is developed.

→ for an emitter follower, voltage gain is almost unity. Therefore the Output voltage is also ramp voltage.

→ ∴ Thus the bootstrap circuit Generates a ramp voltage.



t_p = pluse width

T_s = Sweep time

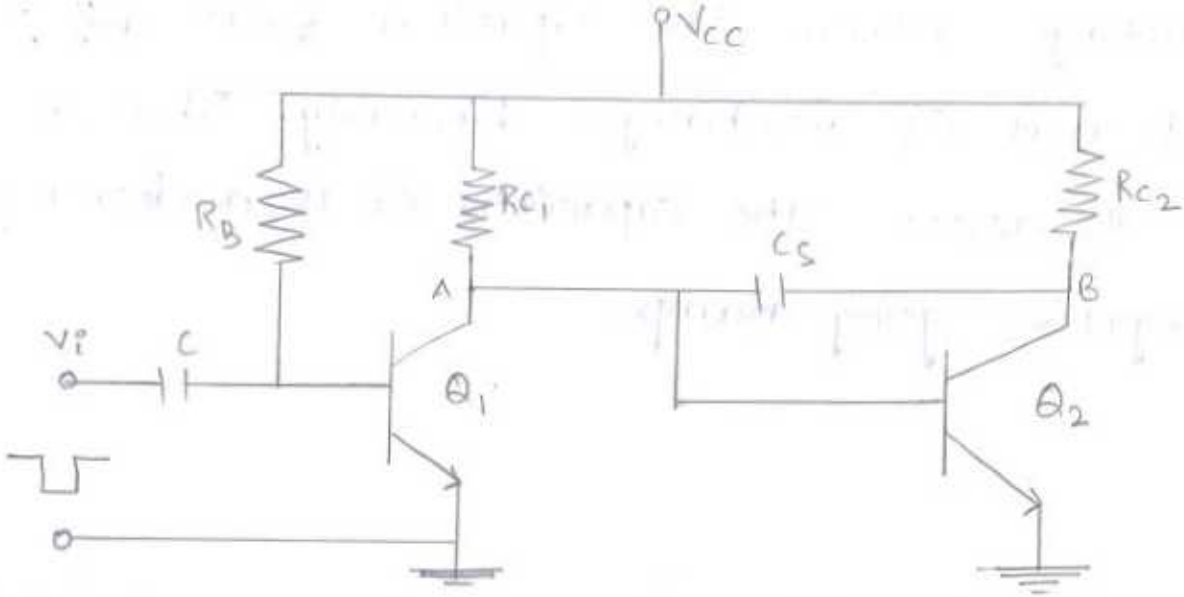
T_r = Return time = $\frac{T_s}{10}$.

$RC_1 = C_s = T_s$

2.4 Transistor Miller Time Base Generator

*(Miller Sweep circuit:)

→ Miller Sweep circuit Generates a ramp voltage using basic principle of Bootstrap sweep Generator. Here, in Miller Sweep circuit Generates a negative Ramp. And Also makes use of a high gain amplifier and it negative feed back.



Switch ← | → High Gain amplifier.

→ Transistor Q_1 acts as ON-OFF switch, and Q_2 is a high gain amplifier.

→ The input V_i is a pluse or rectangular voltage.

→ When the input V_i is positive, Q_1 is ON in Saturation. V_A becomes zero. $\therefore V_A = V_{CE}(sat) = 0$

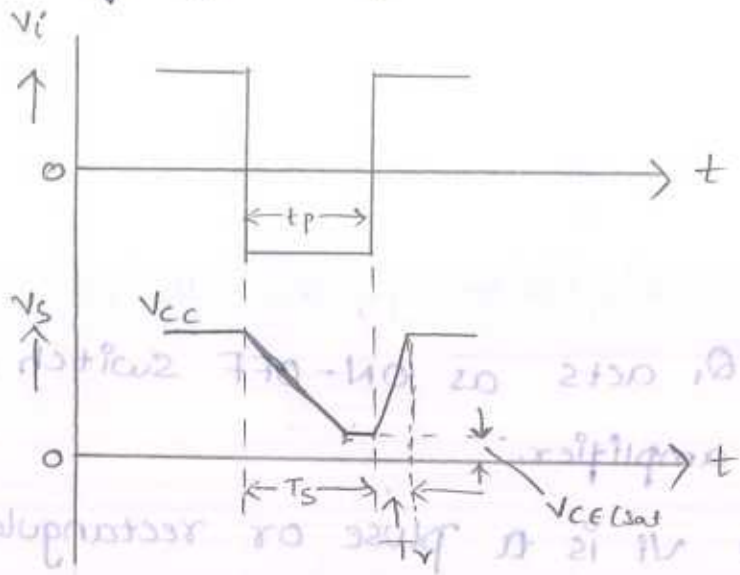
→ Transistor Q_2 remains OFF, (∵ it cannot get the necessary base drive) $\therefore C_S = V_{CC}$

→ When the input V_i goes negative, Q_1 cannot conduct. with Q_1 OFF 'A' tends to rise to V_{CC}.

→ But, due to 'Cs' present in the circuit, 'V_A' cannot rise to V_{CC} instantaneously.

→ with Q_1 OFF and A goes up, Q_2 becomes ON. The potential of B tends to decrease to zero, but due to Cs; V_B [illegible] So, V_A gradually increases and V_B gradually decreases.

→ The voltage across the capacitor falls. The Result is that C_s discharges linearly. Thus the voltage V_s across the capacitor C_s is a decreasing. i.e, Negative going Ramp.



$T_s \leq t_p$

$T_s = R_{c_1} C_s$

$T_r = R_{c_2} C_s$

4.2.5

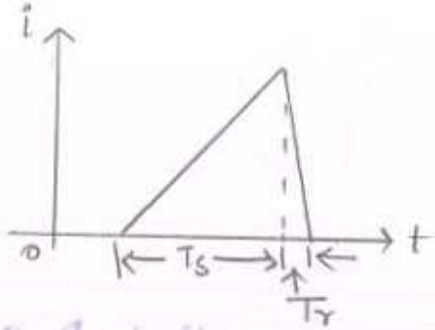
* Comparison between Miller and Bootstrap Sweep ckt:-

Bootstrap Sweep circuit.	Miller Sweep circuit
→ In bootstrap Sweep circuit the the polarity of Sweep voltage is positive.	→ In Miller Sweep circuit the Polarity of Sweep voltage is negative.
→ Non inverting amplifier is used.	→ Inverting amplifier is used.
→ The open circuit gain of the amplifier. is $A = +1$.	→ The open circuit gain of the amplifier is $A = -\infty$.
→ The Linearity of the Sweep voltage is poor	→ The Linearity of the Sweep voltage is better
→ A voltage Source V is Simulated like that V is always equal to the instantaneous capacitor voltage VC.	→ A voltage Source is like that which is never equal to the immediate capacitor voltage Vc.

*4.2.6 Current Time - Base Generators :-

→ If a constant current is passed through a capacitor, the voltage across the capacitor is a ramp. $V_c = \alpha t$.

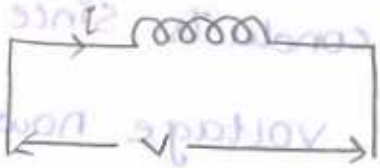
→ If this ramp voltage is applied to fixed resistor, obviously the current which results is a ramp current.



T_S = Sweep Time
T_r = Return time.

4.2.6.1 Generating of current Ramp :-

→ If a constant voltage is maintained across an Inductor, the current which flows through the Inductor is ramp.



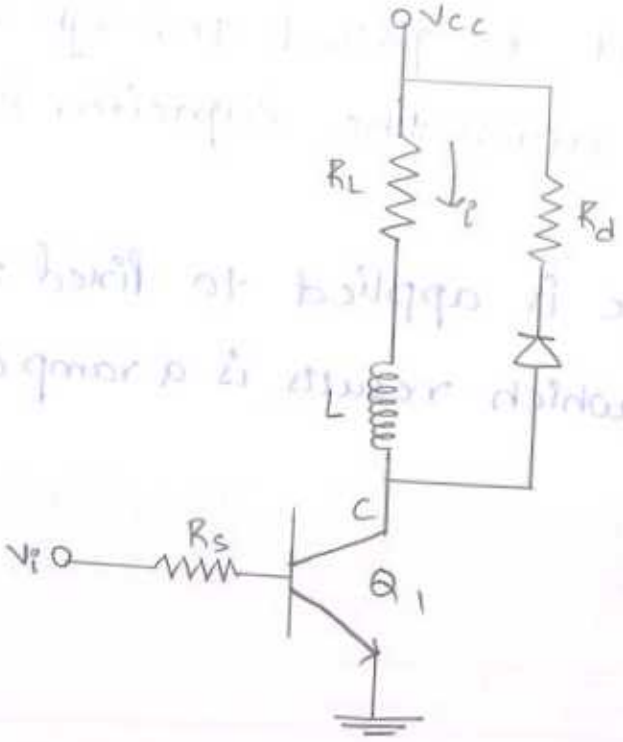
$$i = \frac{1}{L}\int V\,dt$$

→ Let coil of Inductance 'L' Henry, a voltage V be applied across it, 'i' is resulting current.

$$i = \frac{V}{L}\int dt = \left(\frac{V}{L}\right)t \rightarrow \alpha t \quad \left(\because \alpha = \frac{V}{L}\right).$$

→ Since, both V and L are constant in magnitude, i is proportional to t. Hence the current in the Inductor is a ramp.

2.6 Basic current Sweep circuit :-



→ An inductor, shunted by a diode D and resistor R_d is connected in between the voltage source Vcc and the collector of a transistor Q.

→ When the input signal is pulse of negative, Q_1 is OFF and the current $i = 0$.

→ when pulse is positive Q_1 conducts since it is ON, Diode is forward biased. The voltage now becomes Vcc.

→ Applying KVL to circuit

$$L\frac{di}{dt} + iR_L = V_{cc}$$

$$\frac{di}{dt} + \left[\frac{1}{\tau}\right] i = a, \quad \left[\because \tau = \frac{L}{R_L}\right] \& \left[a = \frac{V_{cc}}{L}\right].$$

→ The solution is of form $i = CF + PI$ [diff equation]

$$i = K_1 e^{-t/\tau} + a\tau$$

where $\boxed{\tau = \frac{L}{R_L}}$

→ By evaluating K_1 ; at $t=0$; $i=0$.

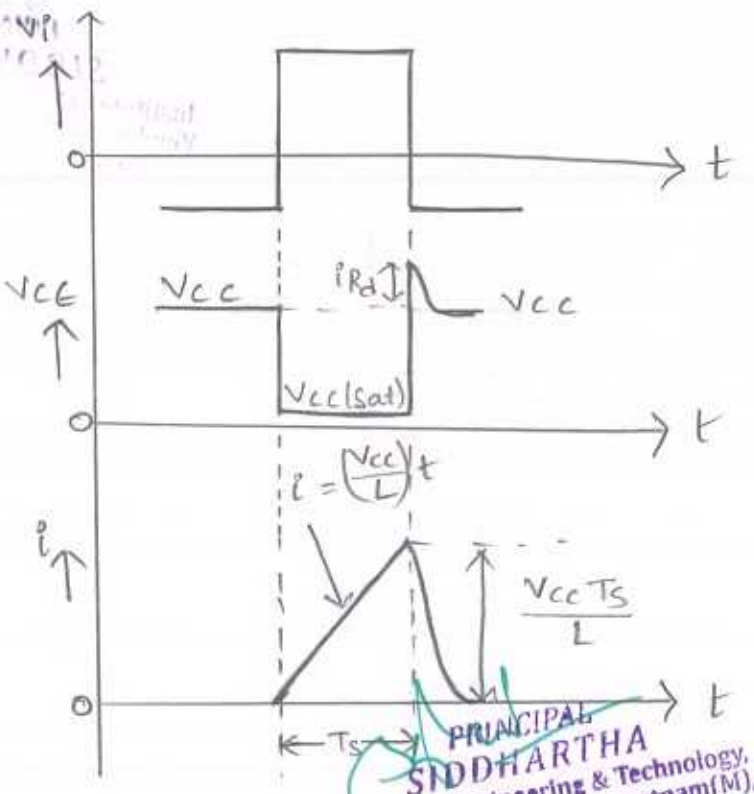
$$K_1 = -a\tau$$

$$\therefore \quad i = a\tau\left(\frac{t}{\tau}\right)$$

$$i = at$$

$$\boxed{i = \left[\frac{V_{cc}}{L}\right]t} \rightarrow \text{current is a ramp.}$$

→ The input voltage and inductor current wave forms are shown below.



4.2.7 Methods of Linearity Improvement :-

* Compensation Circuit is Used to improve the Linearity of the time base generators like Bootstrap or Millersweep time Base generators.

* And Use Inductor Circuit, Linear Capacitor Charging is achieved by ; RLC Series Circuits

PRINCIPAL
SIDDHARTHA
Institute of Engineering & Technology,
Vinobha Nagar(V), Ibrahimpatnam(M),
Ranga Reddy District-501 506.

5-1 Sampling Gates & UNIT - IV

1.1 Basic operating principles of Sampling Gates :-

The basic operating principle of a sampling gate is illustrated in figures (a) and (b).

In fig (a) the switch is normally open, but is in closed position when the signal is transmitted.

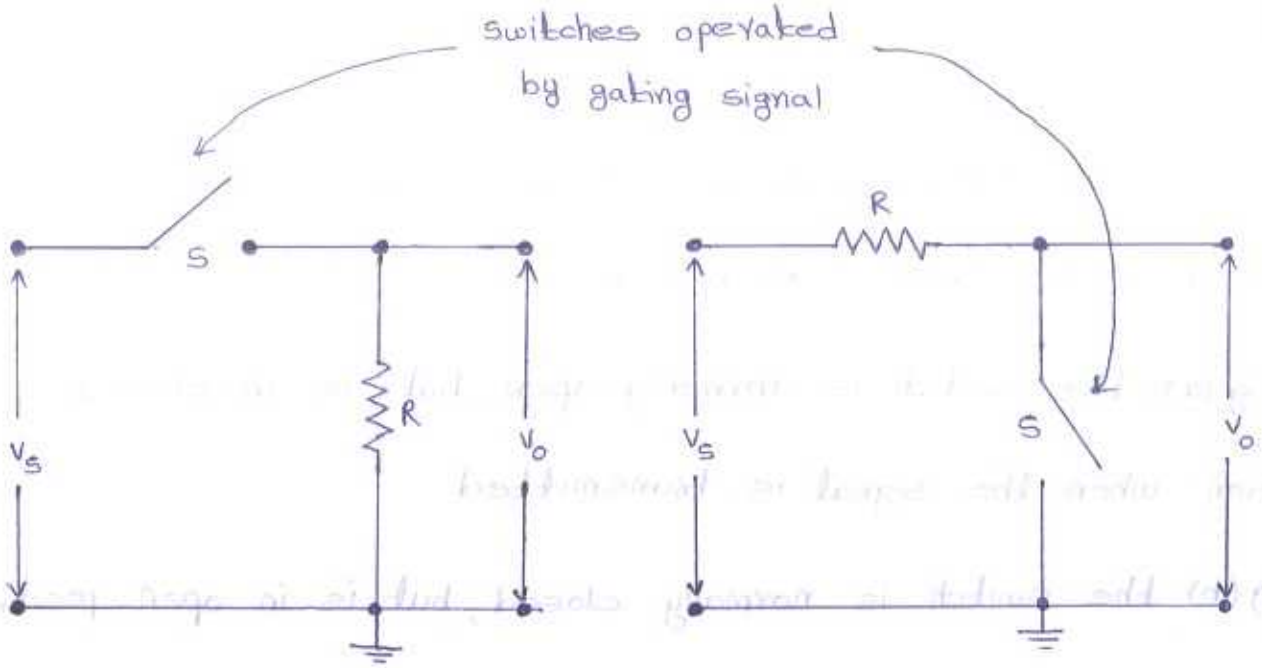
In fig (b) the switch is normally closed, but is in open position when the signal transmitted.

These switches are normally electronic devices - diodes or transistors

When the device is conducting, it acts as a closed switch and when it is not conducting it acts as an open switch.

Ideally, a closed switch should have zero resistance and an open switch should have infinite resistance, but semiconductor devices do not have infinite back resistance and their forward resistances may lie in the range of several ohms.

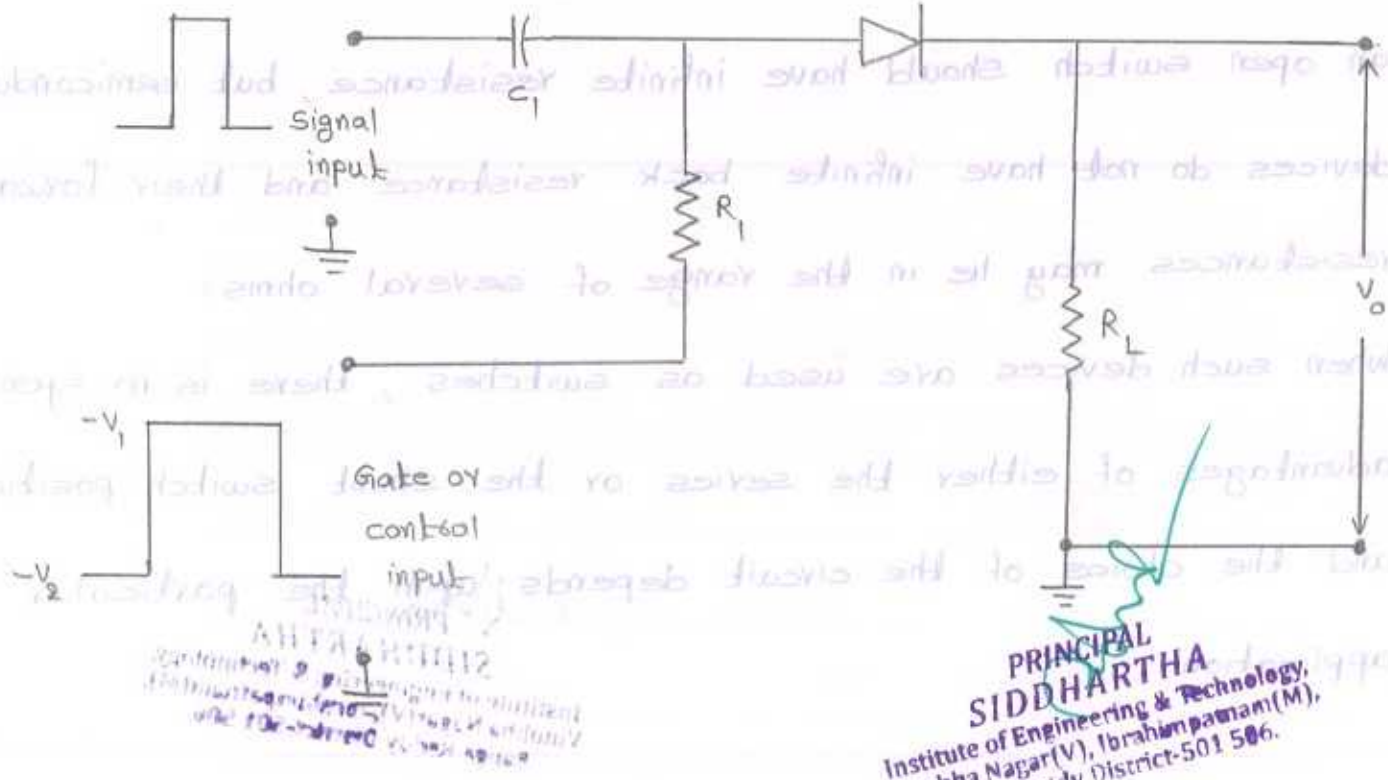
When such devices are used as switches, there is no specific advantages of either the series or the shunt switch position and the choice of the circuit depends upon the particular application.



A samping gate using (a) series switch (b) shunt switch

1.2 Unidirectional Diode Gate :-

A unidirectional diode gate which transmits only the positive-going input signals is shown in figure.



A unidirectional diode gate

The gate signal i.e the signal which determines the gating or transmission period is a rectangular waveform that makes abrupt transitions between the two negative level $-V_1$ and $-V_2$.

The gate signal is also called a control pulse, a selector pulse, or an enabling pulse.

When the gating signal is at its lower level $-V_2$, the diode is heavily back biased and there will be no output due to the input signal unless the peak amplitude of the input signal is larger than the magnitude of this back-biasing voltage.

When the gate signal is at its upper level $-V_1$, a time-coincident signal input pulse may be transmitted to the output.

The effect of the upper level of the gating signal on the output is illustrated in figure

The input signal is a +10V pulse.

In figure (a), when the gate pulse has $-V_2 = -20\,V$ and $-V_1 = -10\,V$, there is no output pulse at all.

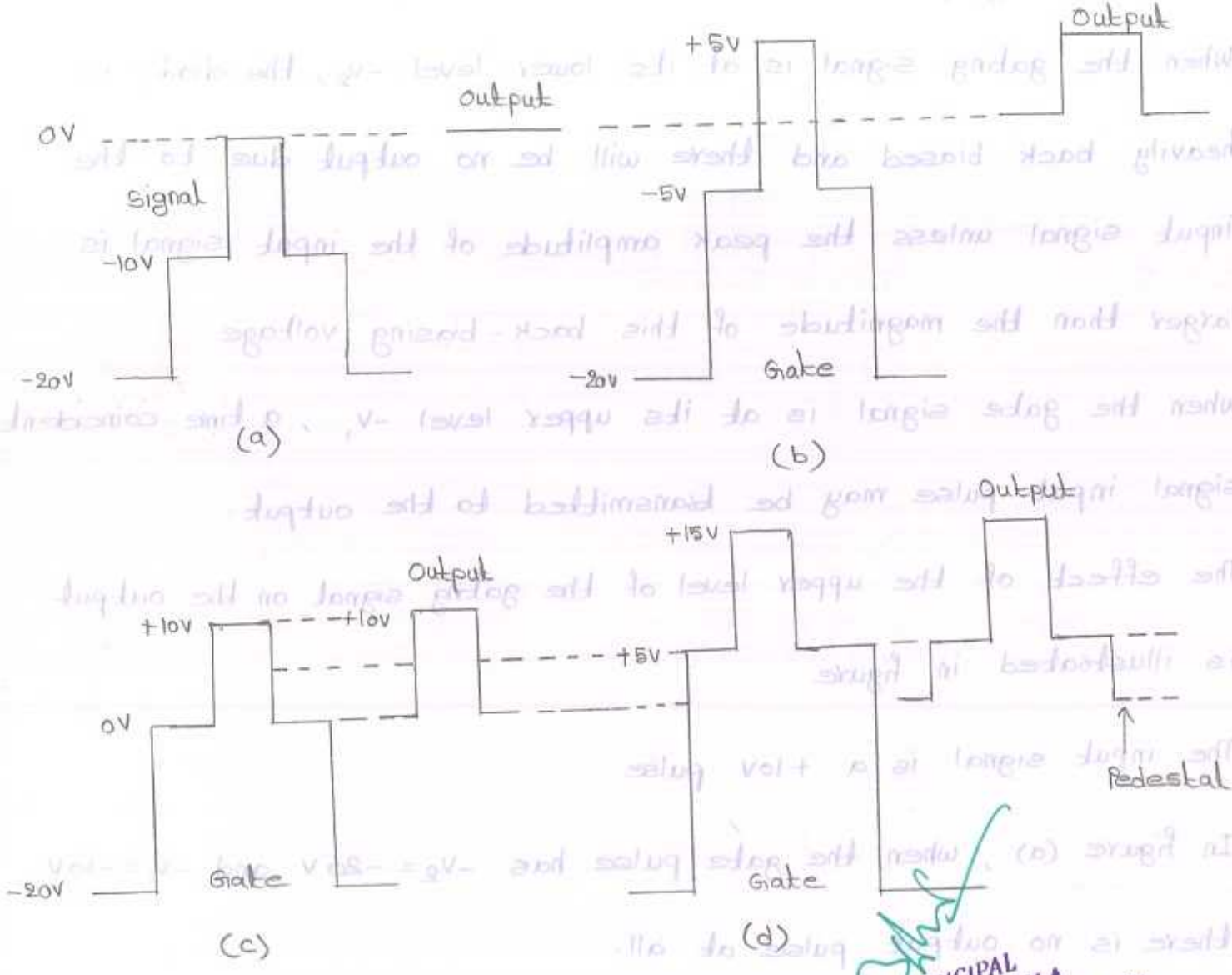
In figure (b), when $-V_2 = -20V$ and $-V_1 = -5V$, the output is a $+5V$ pulse.

In figure (c), when $-V_2 = -20\,V$ and $-V_1 = -10\,V$, the output is a +10V pulse.

In figure (d), when $-V_2 = -20V$ and $-V_1 = 5V$, the output is a 10V pulse

superimposed on a pedestal of +5V.

Actually the waveforms with vertical edges shown in figure are unrealistic because the R_1C_1 network constitutes an integrating network for the gate waveform and therefore the gating signal will have exponentially rising and falling edges as shown in figure (e).

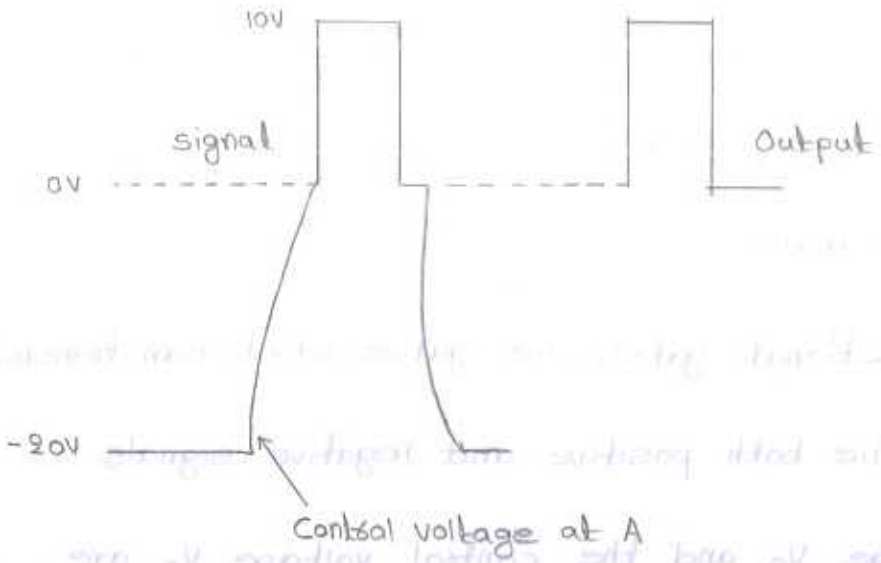


Illustrating the effect of control voltage (-V) on the output

Hence this type of gate is not suitable for transmitting a portion of a continuous waveform.

However if the input is a pulse of very short duration compared

to the gate width, the input may be transmitted satisfactorily.



(e) Distortion of the control waveform

Advantages of the unidirectional diode gate :-

i) It is extremely simple.

ii) There is very little time delay through the gate.

iii) The gate draws no current in its quiescent condition.

iv) The gate can be easily extended into a multi-input OR circuit, with an INHIBITOR or NOT terminal.

Disadvantages of the unidirectional diode gate :

i) There will be interaction between the signal source and the control voltage source.

ii) The gate is of limited use because of the slow rise of the control voltage at the diode.

Bidirectional Sampling Gates Using Transistors :

All the gates discussed so far have a limitation that they transmit signals of only one polarity i.e either only positive signals or only negative signals.

Fig (a) and (b) show bidirectional gates, i.e gates which can transmit signals of either polarity i.e both positive and negative signals.

In fig (a), the signal voltage V_s and the control voltage V_c are applied through the summing resistors R_1 and R_2 to the base of a transistor.

The gating voltage V_c is a pulse waveform between the levels V_1 and V_2 and with a pulse width t_p equal to the desired transmission interval.

When the gating signal is at its lower level V_2, the transistor is well below cut-off.

When the gating signal is at its upper level V_1, the bias brings the transistor into the active region.

So, as long as the gating signal is at its upper level, signals of either polarity appearing at the base will be sampled and will appear amplified at the output.

Hence the circuit of figure (a) act as a bidirectional gate.

Diodes D_1 and D_2 prokeck Q_1 from being damaged by the negative spikes of voltages at the inputs.

When negative spikes appear at the input kerminals, the diodes conduct and bypass the spikes to ground.

Diode D ensures that Q_3 and Q_4 do not conduct simultaneously.

Transistor Q_3 acts as an emitter follower.

When both the inputs A and B are high (+5v), both the base-emitter junctions of Q_1 are reverse biased, so no current flows to the emitters of Q_1. However, the collector-base junction of Q_1 is forward biased. So a current flows through R_1 to the base of Q_2, and Q_2 turns on. Current from Q_2's emitter flows into the base of Q_4. So, Q_4 is turned on.

The collector current of Q_2 flows through R_2 and, so, produces a drop across it thereby reducing the voltage at the collector of Q_2. Therefore Q_3 is OFF. Since Q_4 is ON, V_o is at its low level ($V_{CE\,sat}$). So, the output is a logic 0.

When either A or B or both are Low, corresponding base-emitter junction(s) is are forward biased and the collector-base junction of Q_1 is reverse biased. So, the

current flows to ground through the emitters of Q_1.

Therefore, the base of Q_1 is at 0.7 V, which cannot forward bias the base-emitter junction of Q_2, so, Q_2 is OFF.

With Q_2 OFF, Q_4 does not get the required base drive. So, Q_4 is also OFF. Transistor Q_3 gets enough base drive because Q_2 is OFF, i.e. since no current flows into the collector of Q_2, all the current flows into the base of Q_3, and therefore, Q_3 is ON.

The o/p voltage, $V_o = V_{cc} - V_{R_2} - V_{BE_3} - V_D$

$\simeq 3.4$ to 3.8 V

which is a logic High level.

So the circuit acts as a two-input NAND gate.

PRINCIPAL
SIDDHARTHA
Institute of Engineering & Technology,
Vinobha Nagar(V), Ibrahimpatnam(M),
Ranga Reddy District-501 506.

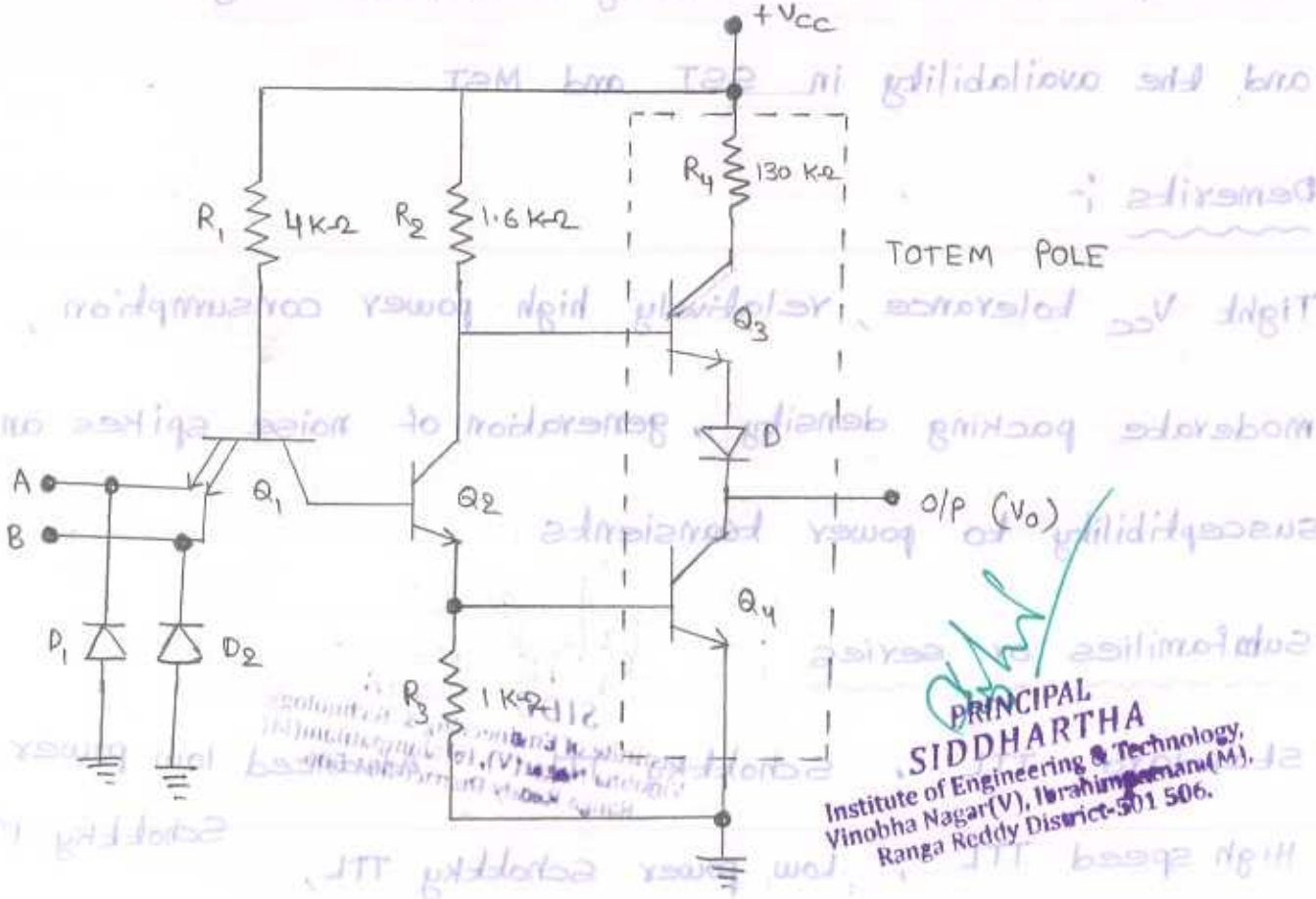
2.42 Standard TTL (Two - Input TTL NAND Gate) :-

For standard TTL, 0V to 0.8 V is treated as a logic 0 and 2V to 5V is treated as logic 1.

In the circuit of the two-input TTL NAND gate shown in figure, the input transistor Q_1 is a "multiple emitter transistor".

Transistor Q_2 is the called the "phase splitter".

Transistor Q_3 sits above, Q_4 and, therefore, Q_3 and Q_4 make a totem pole arrangement.



TTL NAND Gate

3.2.4 Transistor Transistor Logic (TTL) :

The TTL or T^2L family is so named because of its dependence on transistors alone to perform basic logic operations.

It is the most popular logic family.

It is also the most widely used bipolar digital IC family.

The TTL uses transistors operating in saturated mode.

The basic TTL logic circuit is the NAND gate.

Merits :-

Good speed, low manufacturing cost, wide range of circuits, and the availability in SSI and MSI.

Demerits :-

Tight V_{cc} tolerance, relatively high power consumption, moderate packing density, generation of noise spikes and susceptibility to power transients.

Subfamilies or series :-

Standard TTL, Schottky TTL, Advanced low power Schottky TTL, High speed TTL, Low power Schottky TTL, Fast TTL, Low power TTL, Advanced Schottky TTL,

hence no voltage drop occus across R.

The output voltage $X = +5V$ (logic 1).

b) when $A = +5V$, T is ON. Current flows through R and hence almost all the supply voltage is dropped across R.

The output voltage $X = V_{CE}(sat) = 0.3V \simeq 0V$ (logic 0)

The truth table for the NOT gate is shown below.

Input	Output
A	X
Low	High
High	Low

Input	Output
A	X
0	1
1	0

The Ic 7404 contains six NOT gates.

2.4 Comparision of Logic Families :-

Logic Family	Propagation delay time (ns)	Power dissipation per gate (mw)	Noise Margin (V)	Fan-in	Fan-out	Cost
TTL	9	10	0.4	8	10	Low
ECL	1	50	0.25	5	10	High
Mos	50	0.1	1.5			Low
CMos	<50	0.01		10	50	Low
IIL	1	0.1	0.35	5	8	Very Low

passes through them. T_3 gets enough base drive from +5 V source and so goes into saturation.

Output $X = V_{CE}(sat) = 0.3V \simeq 0V$ (logic 0).

d) when A = 5 V and B = 5 V, both T_1 and T_2 are ON. Current flows through them. T_3 does not get enough base drive and so will be OFF.

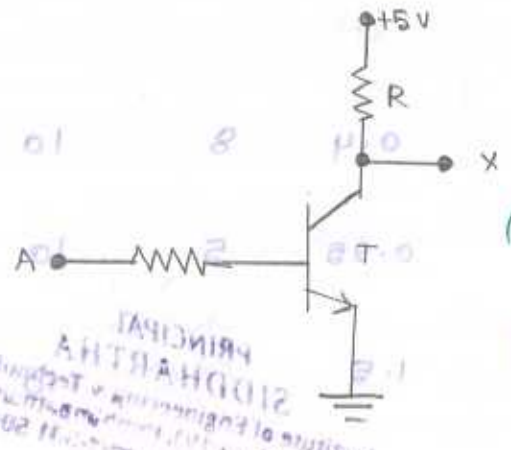
Output X = 5V (logic 1).

The IC 7408 contains four two-input AND gates, the IC 7411 contains three three-input AND gates, and the IC 7421 contains two four-input AND gates.

2.3 Realization of NOT gate :-

A discrete NOT gate may be realized using a transistor as shown in fig.

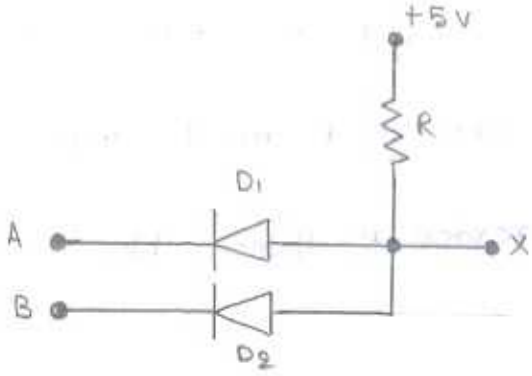
The input to the gate may be 0 V or +5 V.



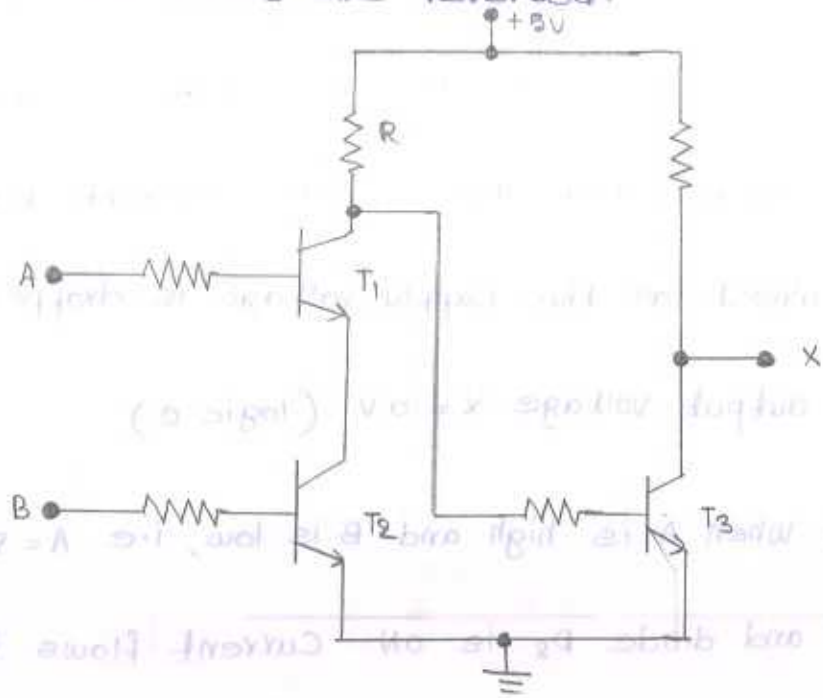
Transistor NOT gate

a) when A = 0V, transistor T is OFF. No current flows through R, and

A negative logic AND gate uses the same configuration as that of figure (a) except that all the diodes are reversed.



a) Two-input diode AND gate (DL AND gate)



b) Two-input transistor AND gate (RTL AND gate)

Discrete AND gates

In the transistor AND gate (RTL AND gate) shown in fig (b).

a) When A = 0 V and B = 0 V, T_1 is OFF and T_2 is OFF. No current passes through them. T_3 gets enough base drive from +5V source and so goes into saturation.

Output $x = V_{CE}(sat) = 0.3V \simeq 0V$ (logic 0).

b) When A = 0 V and B = 5 V, both T_1 and T_2 are OFF. No current passes through them. T_3 gets enough base drive from +5 V source and so goes into saturation.

Output $x = V_{CE}(sat) = 0.3V \simeq 0V$ (logic 0).

c) When A = 5V and B = 0 V, both T_1 and T_2 are OFF. No current

and so almost all the supply voltage is dropped across R.

Hence the output voltage X = 0 V (logic 0).

b) when A is low and B is high i.e A = 0 V and B = 5V, diode D_1 is ON and diode D_2 is OFF. Current flows through R and D_1 and almost all the supply voltage is dropped across R. Hence the output voltage X = 0 V (logic 0)

c) When A is high and B is low, i.e A = 5 V and B = 0 V, diode D_1 is OFF and diode D_2 is ON. Current flows through R and D_2 and almost all the supply voltage is dropped across R.

Hence the output voltage X = 0 V (logic 0).

d) When both A and B are high, i.e A = 5 V and B = 5V, both the diodes D_1 and D_2 are OFF. No current flows through R, so no voltage drop across R.

Hence the output voltage X = 5 V (logic 1).

The truth table for the above diode logic AND gate is shown below.

Truth table

Inputs		Output
A	B	X
Low	Low	Low
Low	High	Low
High	Low	Low
High	High	High

Truth table

Inputs		Output
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

c) when A = 5 V and B = 0 V, T_1 is ON and T_2 is OFF. Current flows through T_1, and T_3 does not get enough base drive and so T_3 is OFF. No current flows through its collector resistance R_c. so no voltage drop across it.

The output X = +5V (logic 1).

d) when A = 5 V and B = 5 V, both T_1 and T_2 are ON. Current flows through T_1 and T_2, and T_3 does not get enough base drive and so T_3 is OFF. No current flows through its collector resistance R_c. So no voltage drop across it.

The output X = +5V (logic 1).

The IC 7432 contains four two-input OR gates.

22 Realization of AND gate :-

Discrete AND gates may be realized by using diodes or transistors as shown in fig (a) and fig (b) respectively.

The inputs A and B to the gates may be either 0 V or +5V.

The two inputs A and B can occur in four possible combinations.

In the positive logic diode AND gate (Diode Logic AND gate) shown in fig (a) A and B are voltage sources and R is load resistance.

a) when both A and B are low, i.e A = 0 V and B = 0 V, both the diodes D_1 and D_2 are ON. Current flows through R, D_1 and D_2

The truth table for the above two input diode OR gate is shown below:

Truth Table

Inputs		Output
A	B	X
Low	Low	Low
Low	High	High
High	Low	High
High	High	High

Truth Table

Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

A negative logic OR gate uses the same configuration as that of fig (a) except that all the diodes are reversed.

In the transistor OR gate (RTL OR gate) shown in fig (b).

a) When A = 0 V and B = 0 V, both T_1 and T_2 are OFF. No current flows through them.

T_3 gets enough base drive from the +5V supply and so T_3 is ON and the output $X = V_{CE}(sat) = 0.3\,V \simeq 0\,V$ (logic 0).

b) When A = 0 V and B = 5 V, T_1 is OFF and T_2 is ON. Current flows through T_2, and T_3 does not get enough base drive and so T_3 is OFF. No current flows through its collector resistance R_C. So there is no voltage drop across it.

The output X = +5 V (logic 1).

In the positive logic diode OR gate (Diode Logic OR gate) shown in figure (a) A and B are voltage sources and R is load resistance The two inputs A and B can occur in four possible combinations

a) When both A and B are low, i.e when A = 0 V and B = 0 V, both the diodes D_1 and D_2 are OFF. No current flows through R, and so, no voltage drop occurs across R. Hence, the output voltage X = 0 V (logic 0).

b) When A is high and B is low, i.e A = +5V and B = 0 V, diode D_1 is forward biased and diode D_2 is reverse biased. Current flows through D_1 and R and the output voltage X = 5V (logic 1).

c) When A is low and B is high, i.e A = 0 V and B = +5V, diode D_1 is OFF and diode D_2 is ON. Current flows through D_2 and R and the output voltage X = 5V (logic 1)

d) When A is high and B is high, i.e A = +5V and B = +5V both the diodes D_1 and D_2 are ON. Current flows through D_1, D_2 and R and the output voltage X = +5V (logic 1).

In practice X = 5 V - diode drop = 5V - 0.7V = 4.3 V

which is regarded as logic 1.

following drawbacks

i) If the gating waveforms have definite rise and fall times, two sharp spikes are generated at the output.

ii) There is a continuous flow of current through R_c and so it has to dissipate a lot of heat.

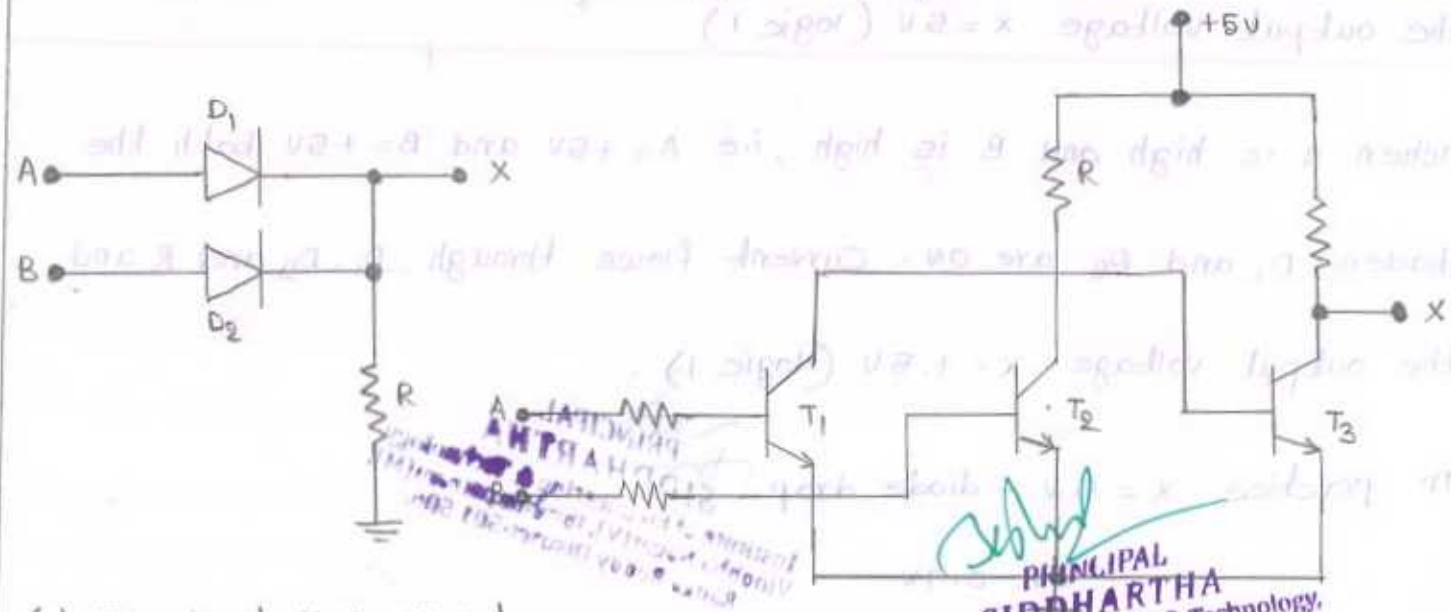
iii) The circuit is complicated. It requires two bias voltages, i.e $-V_{BB_1}$ and $-V_{BB_2}$ and two control signal sources which are complements of each other.

5.2: Realization of Logic Gates Using Diodes & Transistors

2.1 Realization of OR gate :-

Discrete OR gates may be realized by using diodes or transistors as shown in fig (a) and fig (b) respectively.

The inputs A and B to the gates may be either 0 V or +5 V.



(a) Two-input diode OR gate (DL OR gate)

(b) Two-input transistor OR gate (RTL OR gate)

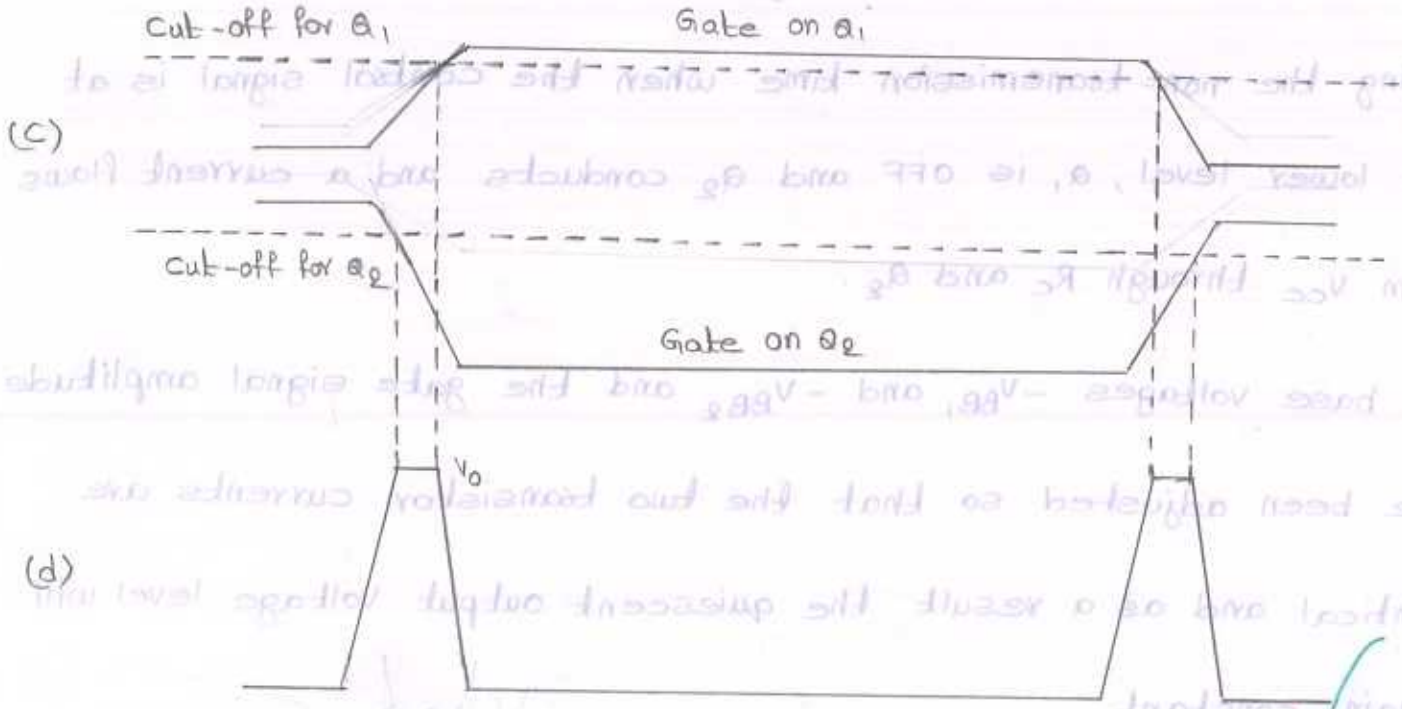
Discrete OR gates

not conducting is biased far below cut-off.

Then when the gate voltage appears, Q_2 will be driven to cut-off before Q_1 starts to conduct, whereas at the end of the gate, Q_1 will be cut-off before Q_2 starts to conduct.

Hence as a result of the gate signals themselves the output will appear as in figure (d).

The gated signal voltage will appear superimposed on this waveform. If the gate waveform rise time is small compared with the gate duration, these spikes may not be very objectionable.



(c) The gating waveform of fig (b) drawn with non-zero rise time

(d) spikes which may occur in the output circuit due to the gating waveform with non-zero rise time.

The circuit of figure (b) used to eliminate pedestal has the

Fig (b) shows a symmetrical arrangement that suppresses the pedestal to a great extent.

Q_1 is the gating transistor and Q_2 is used to minimize the pedestal.

Gating voltages of opposite polarity are applied to the transistor bases.

During the transmission time t_p, when the control signal is at its upper level, Q_1 conducts and Q_2 is cut-off.

A current flows from V_{cc} through R_c and Q_1.

During the non-transmission time when the control signal is at its lower level, Q_1 is OFF and Q_2 conducts and a current flows from V_{cc} through R_c and Q_2.

The base voltages $-V_{BB_1}$ and $-V_{BB_2}$ and the gate signal amplitude have been adjusted so that the two transistor currents are identical and as a result the quiescent output voltage level will remain constant.

If the gate waveform has a non-zero rise time, the arrangement shown in figure (b) does not completely solve the problem of pedestal.

Assume that the gate pulse is large compared with the active region base-voltage range, so that each transistor, when it is

So the output during the gating interval appears as shown in figure (a) where we see that the sampled portion of the signal is superimposed on a pedestal.

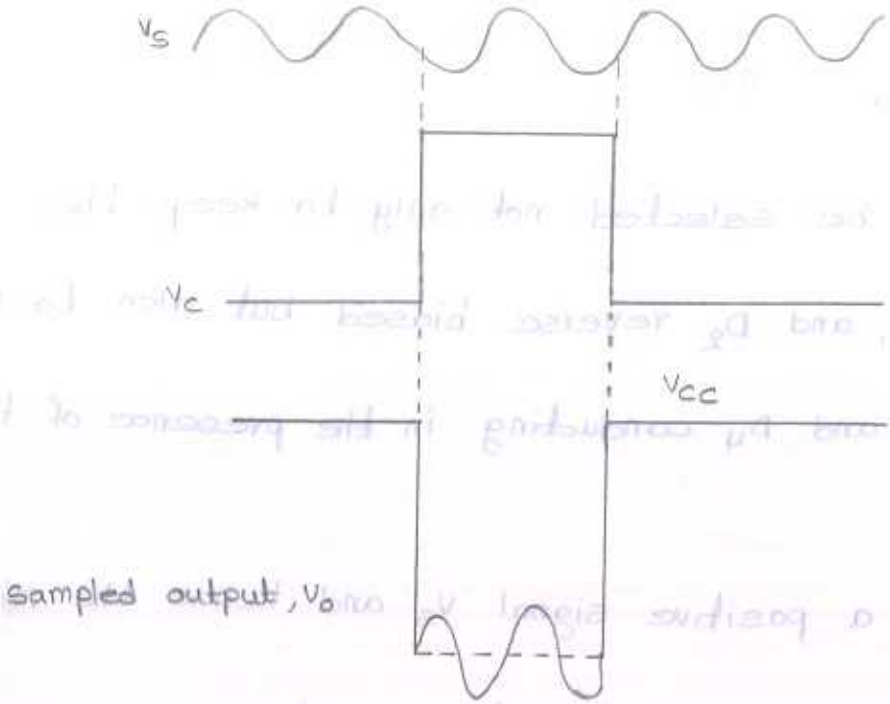


Fig (a) : Pedestal associated with the sampling gates

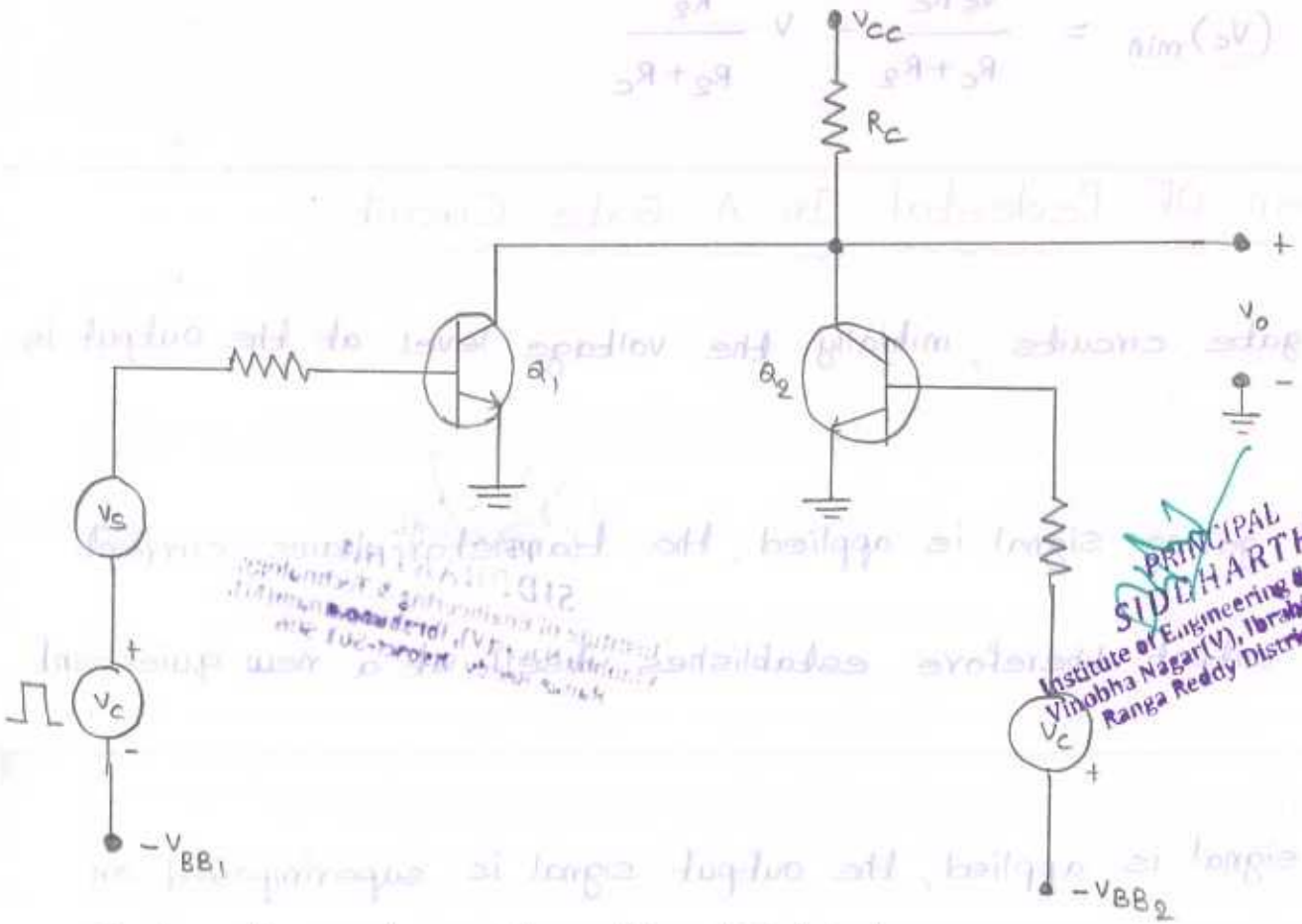


Fig (b) : A sampling gate with provision to cancel the pedestal

V_o given by AV_s where A is the circuit gain.

If the diode D_3 is to continue to be reverse biased, V_c must be at least equal to the voltage at P_1.

Hence,

$$(V_c)_{min} = AV_s$$

The voltage V_n must be selected not only to keep the transmission diodes D_1 and D_2 reverse biased but also to keep the clamp diodes D_3 and D_4 conducting in the presence of the signal V_s.

The voltage at P_2 for a positive signal V_s and hence the minimum value of V_n by applying superposition theorem is

$$(V_c)_{min} = \frac{V_s R_c}{R_c + R_2} - V \cdot \frac{R_2}{R_2 + R_c}$$

16 Reduction Of Pedestal In A Gate Circuit :-

In the gate circuits, initially the voltage level at the output is V_{cc}.

When the gating signal is applied, the transistor allows current and the output therefore establishes at a new quiescent level.

When a signal is applied, the output signal is superimposed on this new quiescent level.

When the control voltages are V_n and $-V_n$, the diodes D_4 and D_3 conduct and the points P_2 and P_1 are clamped to these voltages. So, the diodes D_1 and D_2 are reverse biased.

Under these circumstances, the output is zero.

Let us now compute the gain A and the required minimum values of V, V_c, and V_n.

During transmission, diodes D_3 and D_4 are OFF and the circuite is identical to the B.D.S.G. except that the voltages V_c and $-V_c$ are replaced by $+V$ and $-V$ respectively.

Hence the gain of this circuit is the same as the gain of the gate and is given by

$$A = \frac{R_c}{R_c + R_2} \times \frac{R_L}{R_L + \left(\frac{R_3}{2}\right)}$$

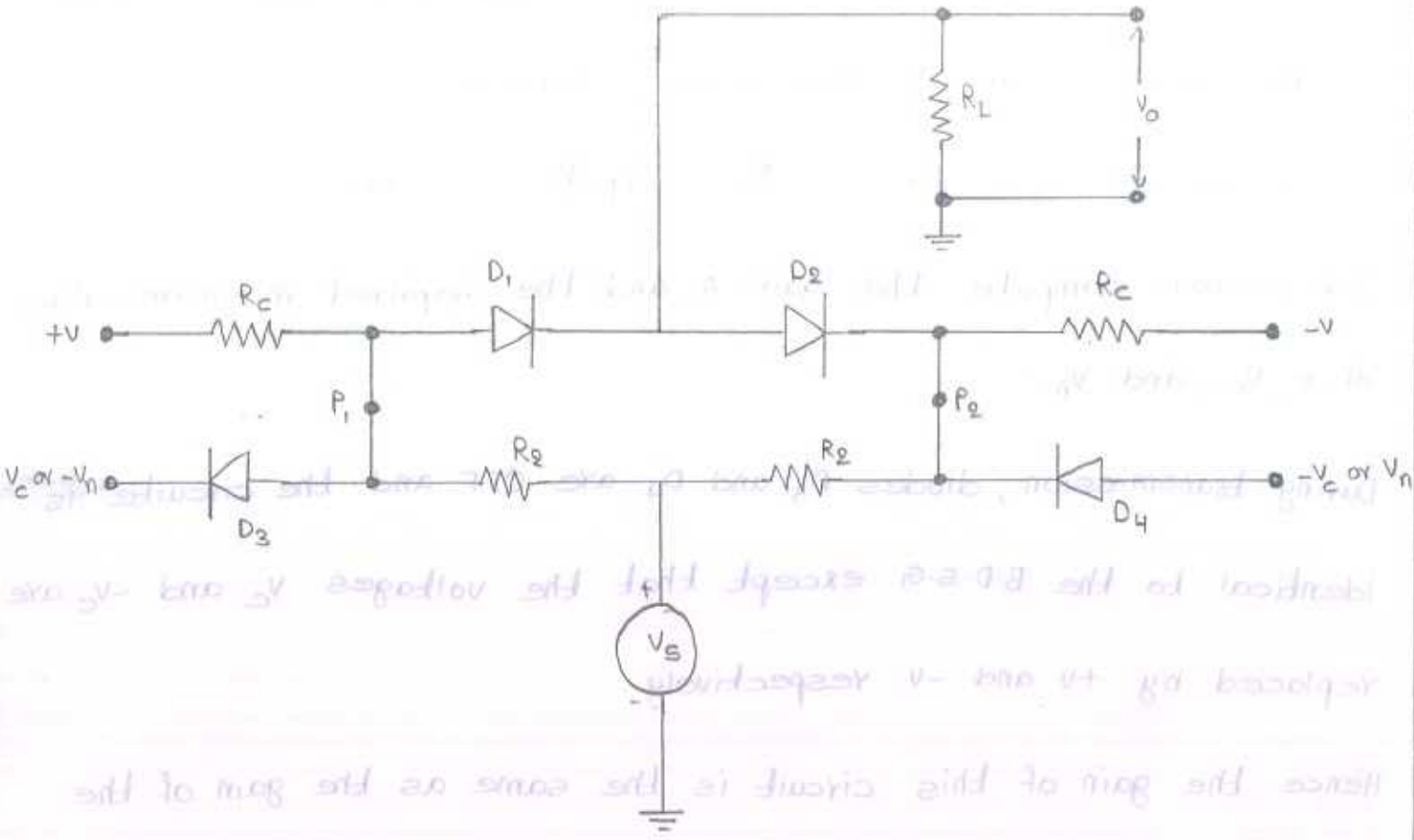
Also, the V_{min} of this circuit is the same as the $(V_c)_{min}$ of the gate of figure of B.D.S.G and is given by

$$V_{min} = \frac{R_c}{R_2} \times \frac{R_3}{R_3 + 2R_L} \times V_S$$

The voltage $(V_c)_{min}$ is computed as follows

Assuming that $R_f << R_L$, for a positive going signal of amplitude V_s, the voltage at point P_1 is the same as the output voltage

Two balanced voltage +V and -V are also required.



A four-diode gate

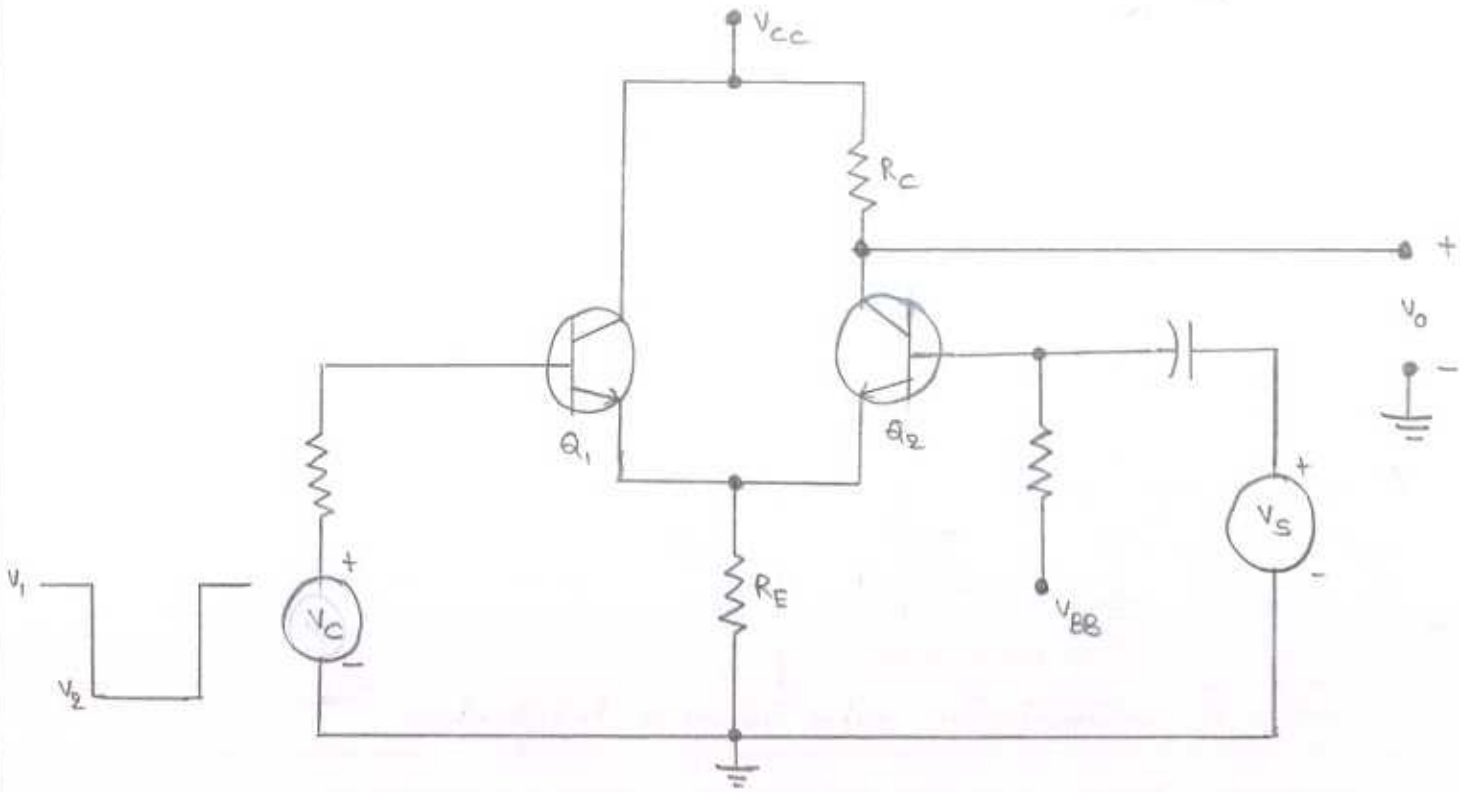
The operation of the four-diode gate is as follows.

When the control voltages are V_c and $-V_c$ respectively, the diodes D_3 and D_4 are reverse biased.

Because of the voltages +V and -V, the diodes D_1 and D_2 conduct and the signal source is coupled to the load through the resistors R_2 and the conducting diodes D_1 and D_2.

Under these circumstances, the control voltage is disconnected from the gate by the reverse-biased diodes D_3 and D_4, so an imbalance in control signals cannot result in a pedestal at the output.

The signal may be applied directly at the base as well



(b) An emitter-coupled bidirectional sampling gate.

Four-Diode Sampling Gate :-

Some of the disadvantages of the two-diode sampling gate are

i) Its gain is low.

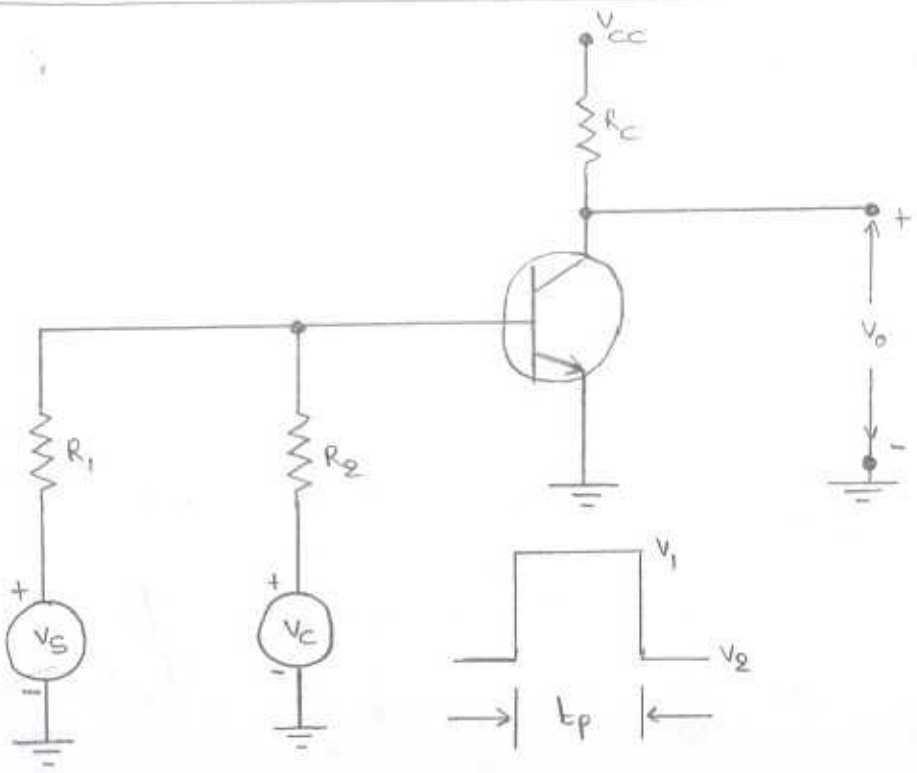
ii) It is sensitive to control voltage imbalance.

iii) There is a possibility that $(V_n)_{min}$ may be excessive.

iv) There may be appreciable leakage through the diode capacitance.

The four-diode sampling gate shown in Figure 4 overcomes these features.

This is obtained by adding two more diodes to the two-diode sampling gate.



(a) A bidirectional gate using a transistor.

Fig (b) shows a bidirectional gate using two transistors which are emitter coupled.

In this, two separate bases are available for the signal and gating voltages

When the gate signal V_c is at its upper level, the transistor Q_1 is ON and the current through R_E is large enough to raise the emitter voltage to the point where Q_2 is cut-off.

With Q_2 cut-off, there is no response at the output for the input signal.

When the control signal V_c is at its lower level, Q_1 is cut off and Q_2 is free to operate as an amplifier stage.

The signal V_s appears at the output amplified.

Capacitor Current

$$i = \frac{dQ}{dt} \qquad Q = C\frac{dV_{in}}{dt}$$

$$i = C\frac{dV_{in}}{dt}$$

$$V_{out} = V_R = R \times i_R$$

$$i_C = C\frac{dV_{in}}{dt}$$

$$i_R = i_C$$

$$\boxed{V_{out} = RC\frac{dV_{in}}{dt}}$$

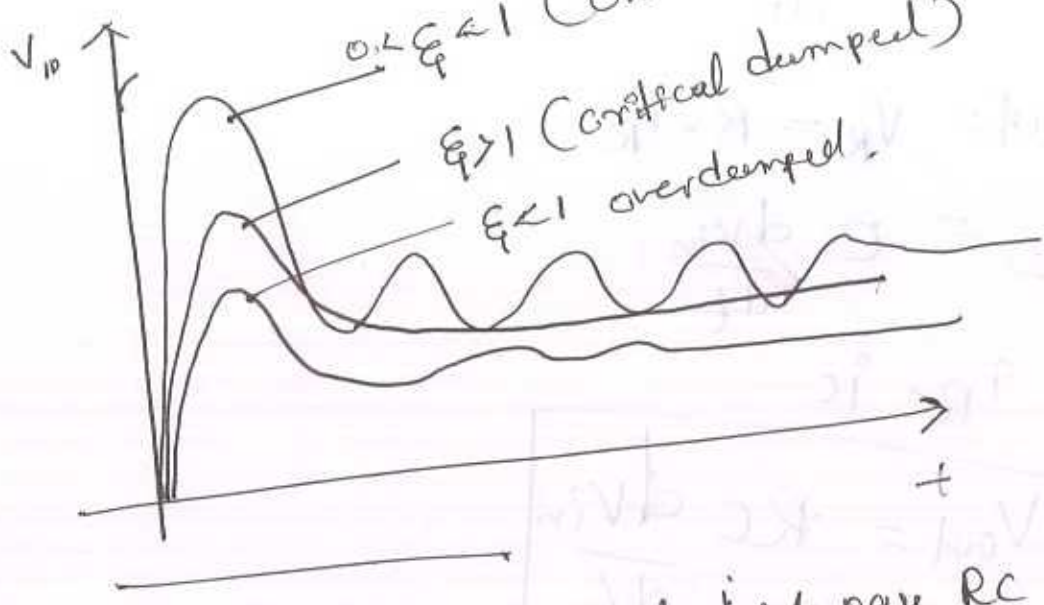
V_{out} is derivative of V_{in}

Step response for critical, over damped cases

$\xi > 1$ → over damped

$0 < \xi < 1$ → Underdamped

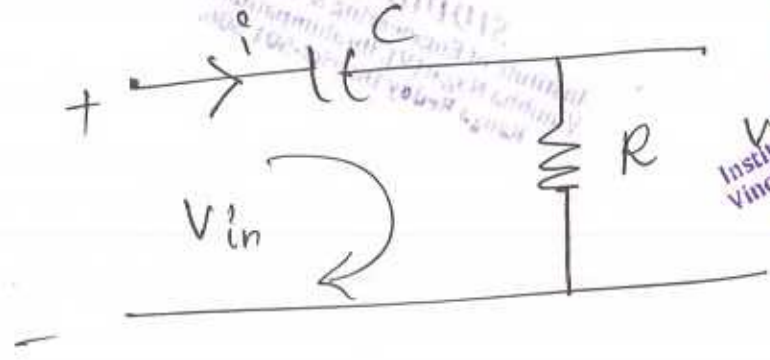
$\xi = 1$ → critical damped



2(b) Explain the working of high pass RC Circuit as a Differentiator?

RC highpass Network working as a differentiator

The Input connected to capacitor and the output taken from across a resistance.



$$\therefore \frac{dv_o}{dt} + \left(\frac{1}{RC}\right) v_o = 0$$

V_o = Complementary function + particular function
(Transient response) + (Steady state response)

The transient response $= Ke^{-t/RC}$

The particular integral represents the steady under this condition the capacitor blocks the passage of "dc" the o/p is zero, Hence the particular integral $= 0$

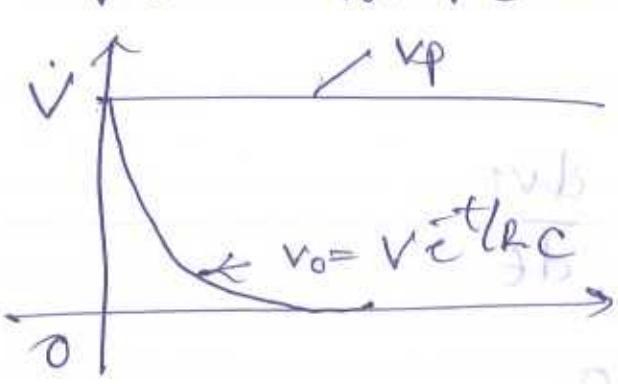
$\therefore V_o = K e^{-t/RC}$ where K is a constant by

Applying Initial Condition

$V_o(0+) = Ke^0 = K$ put $t=0$

But $V_o(0+) = V \quad \therefore K = V$

$V_o = Ve^{-t/RC}$



Subject code: 134CC R16

JNTUH

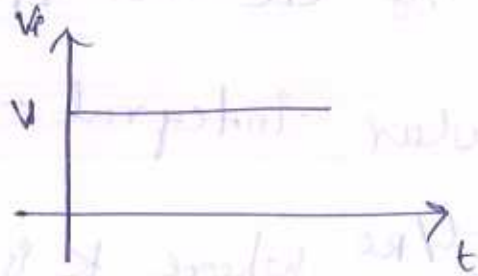
B.Tech II year II Sem Examination, April 2018

Pulse and Digital Circuits

Time 3 Hours Max Marks: 75

2 a) Draw the response of the Circuit for step input Critically damped and over clamped cases for a fixed value of R and C

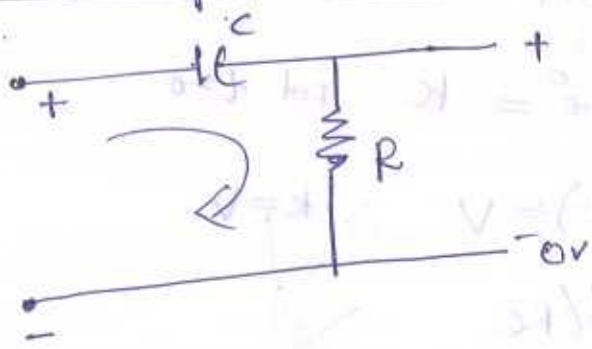
Step Signal



$V_i = V$ for $t > 0$

$V_i = 0$ for $0 < t$

RC high pass Circuit



Apply KCL

$$\left(\frac{1}{RC}\right) V_o + \frac{dv_o}{dt} = \frac{dv_i}{dt}$$

$V_i = V$ for $t \geq 0$

8.a) With the help of neat circuit diagram and waveform ,explain the principle of operation of collector coupled monostable multivibrator.

b) With the help of neat circuit diagram and waveforms, explain the working of a Schmitt trigger. [5+5]

OR

9.a) Draw a simple current sweep circuit and explain its working with the help of diagrams.

b) Draw the circuit diagram and waveforms of a transistor bootstrap time base generator and explain principle of operation. [5+5]

10.a) With help of a neat diagram, explain the working of bidirectional gates using transistors.

b) Draw and explain a diode AND circuit for negative logic and how it works. How an OR circuit acts a buffer circuit? [5+5]

OR

11.a) Compare the performance of various logic families.

b) Explain how to cancel a pedestal in a sampling gate with suitable circuit diagram. [5+5]

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Code No: 134CC

R16

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, April - 2018
PULSE AND DIGITAL CIRCUITS
(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a)	Discuss the response of RC high pass circuit to ramp input voltage.	[2]
b)	Draw the low-pass circuit and explain its working.	[3]
c)	Draw the basic circuit diagram of negative peak clamper circuit.	[2]
d)	Explain the working of an emitter coupled clipper.	[3]
e)	List different switching times of a diode.	[2]
f)	Explain how diode acts as a switch.	[3]
g)	What are the commutating capacitors? Why these are used in binary?	[2]
h)	Write a short note on hysteresis.	[3]
i)	Why totem pole is used in DTL.	[2]
j)	How do sampling gates differ from logic gates?	[3]

PART-B

(50 Marks)

2.a) Draw the response of the circuit for step input critically damped and over damped cases for a fixed value of R and C.
b) Explain the working of high-pass RC circuit as a differentiator. [6+4]

OR

3.a) Define the rise time and write the expression of it.
b) Derive an expression for the output of a high-pass circuit excited by a square input. [4+6]

4.a) Explain the operation of two level slicer.
b) What is meant by comparator? Explain the applications of voltage comparators. [5+5]

OR

5.a) State and prove the clamping circuit theorem.
b) Draw the output waveform of a practical clamping circuit when a square wave is given as input. Derive the relation between Δf and Δr in this case. [5+5]

6. List and explain all the switching times of a transistor. [10]

OR

7.a) Design Transistor switch circuit.
b) Explain in detail about the Silicon-controlled-switch circuits. [5+5]

SIDDHARTHA INSTITUTE OF ENGINEERING &TECHNOLOGY

Vinobha nager ibrahimpatnam..R.R.DistrictHyderabad-501506

II B.Tech. II Sem., Ist Mid-Term Examinations, February – 2019

Branch: ECE **Subject: PDC**

Date: 19-02-19-AN **Objective Exam** **Time: 20min**

Name: A Nagaraj **Hall Ticket No.** 17TP1A04406

Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 10.

I. Choose the correct alternative:

1. The waveform which preserves its form when transmitted through a linear network is a____. [A]

A) Sine wave B) Step signal C) impulse signal D) ramp signal

2. The rise time of the output of a low pass RC circuit is given by [A]

A) 2.2 RC B) 0.35/fH C) 2.2τ D) all the above

3. What is the name of the circuit which converts square wave in to spikes [C]

A) Low pass RC B) Bi stable multi C) High pass RC D) Monoshot

4. When RC high pass circuit act as a differentiator? [A]

A) RC<<T B) RC>>T C) RC=T D) RC=0

5. A circuit that adds positive or negative dc voltage to an input sine wave is called [A]

A) Clamper B) clipper C) diode clamp D) limiter

6. A clamping circuit is also called as _____. [A]

A) Dc restorer B) dc reinserted C) both A and B D) none of the above

7. The upper cut-off frequency of a low pass RC circuit is _____. [C]

A) Zero B) $1/2\pi RC$ C) ∞ D) none of the above

8. What is the response of step input to a high pass RC circuit [A]

A) V e-t/RC B) V (1- et/RC) C) V et/RC D) V (1- e-t/RC)

9. A transistor acts as an amplifier when it is in [C]

A) Saturation region B) Cut-off region C) Active region D) none of the above

10. CRO Probe working as _____ [C]

A) Integrator B) Differentiator C) Attenuator D) none

II. Fill in the Blanks:

11. For DC input signal capacitor C acts as Open Circuit
12. The average value of the output value of an RC high pass circuit is Zero
13. Time constant of RL circuit is $T = L/R$
14. The clamping theorem is given by $V_1/V_2 = R_1/R_2$
15. A network comprising of linear elements is called linear network.
16. In biased clamping a reference voltage source is connected in series with the diode.
17. In a Shunt Clipper, when the diode is OFF, the output follows the input.
18. A circuit which clamps the negative peak of a signal to zero level is called positive biased clamper
19. Rise time is defined as the time by the voltage to rise from 0.1 to 0.9 of its final value.
20. Diode applications Rectifiers, Zener diode,

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Vinobha Nagar(V), Ibrahimpatnam(M),
Ranga Reddy District-501 506.

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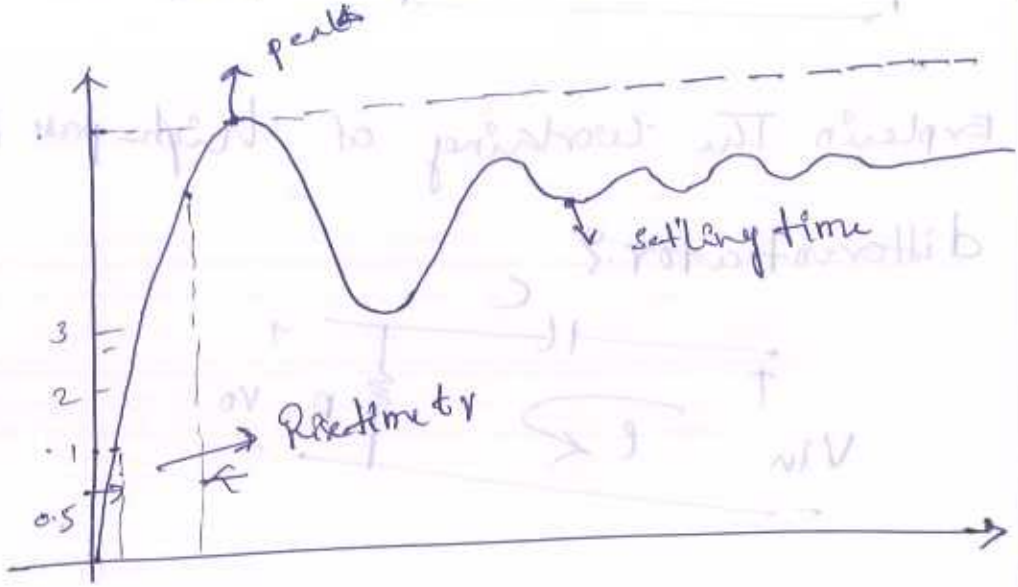
3a) Define the Rise time and write the Expression of it? 5M

The rise time is defined as time required for the signal to make the transition from 10% to 90% of the specified value



$t_r = 2.2RC$

At $t = t_1$, $V_0 = 0.1V$

$\therefore 0.1V = V(1 - e^{-t_1/RC})$

or $e^{-t_1/RC} = 1 - 0.1 = 0.9$

$\therefore t_1 = -RC \log_e 0.9$ ——— (1)

At $t = t_2$ $V_0 = 0.9V$

$\therefore 0.9V = V(1 - e^{-t_2/RC})$

(or) $e^{-t_2/RC} = 1 - 0.9 = 0.1$

(or) $-t_2/RC = \log_e 0.1$

(or) $t_2 = -RC \log_e 0.1$ — (2)

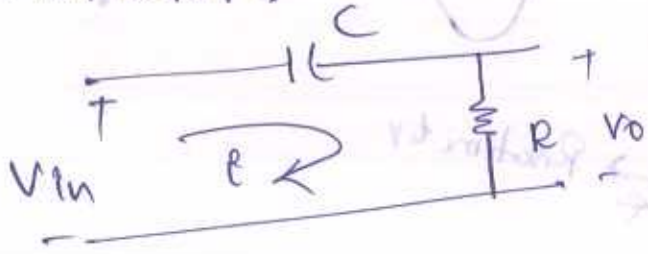
$t_r = t_2 - t_1$

$= -RC(\log_e 0.1 + \log_e 0.9)$

$= 2.2RC$

$\therefore t_r = 2.2RC$

2 b) Explain the working of high-pass RC Ckt as a differentiator?



The above figure behaves as a differentiator

When $RC/T \ll 1$

Apply KVL

$$V_i(t) = v_c(t) + v_R(t) = \frac{1}{C}\int_0^t i(t)\,dt + i(t)R$$

$V_o(t) = V_R(t) = i(t)R$

$V_R(t) \ll V_c(t)$

$$V_i(t) \approx \frac{1}{C}\int_0^t i(t)\,dt$$

Differentiating this equation on either side

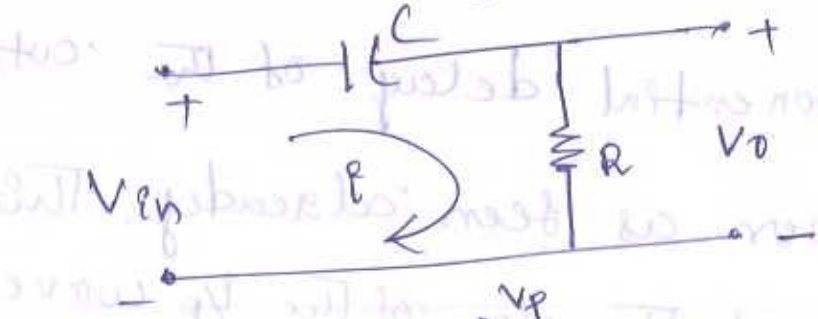
$$\frac{dv_i(t)}{dt} = \frac{1}{C} i(t)$$

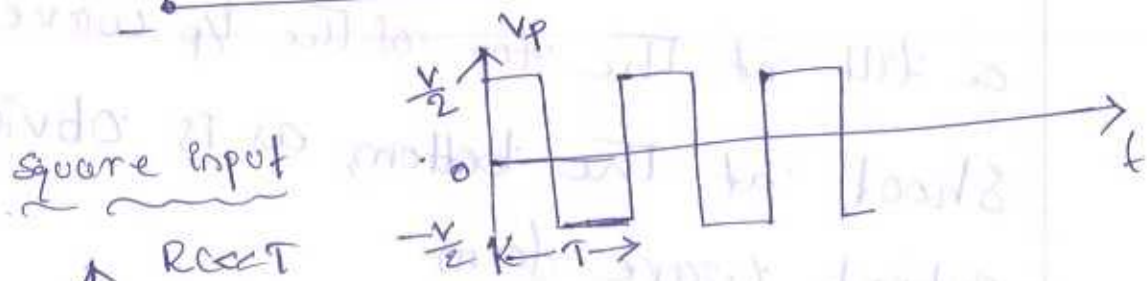
$$i(t) = C \frac{dv_i(t)}{dt}$$

$$\boxed{V_o(t) = RC \frac{dv_i(t)}{dt}}$$

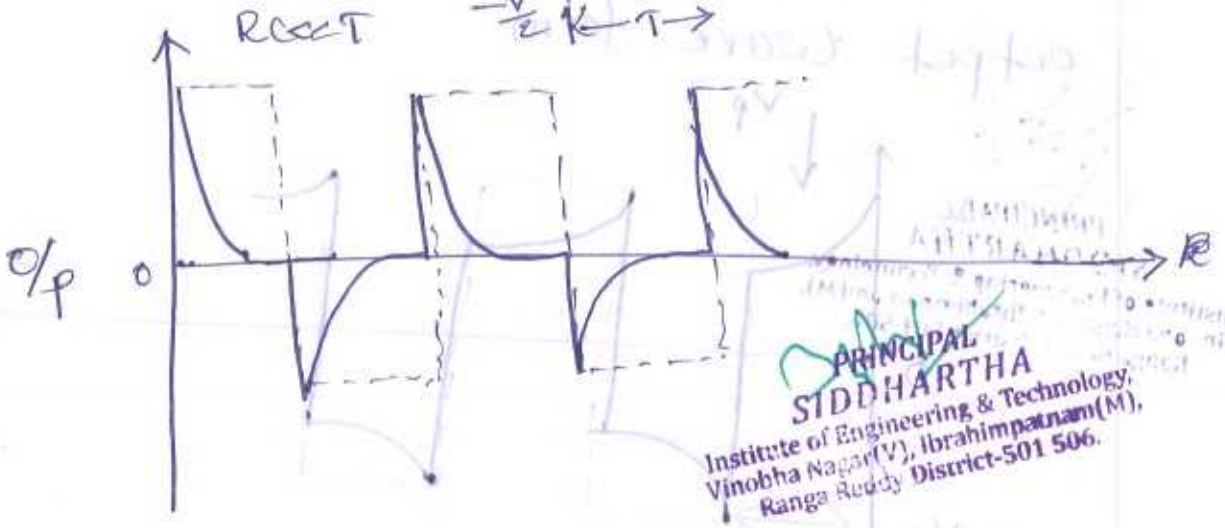
---

3 b) Derive an expression for the output of a high pass Circuit excited by a square input ? 6 M





Square input



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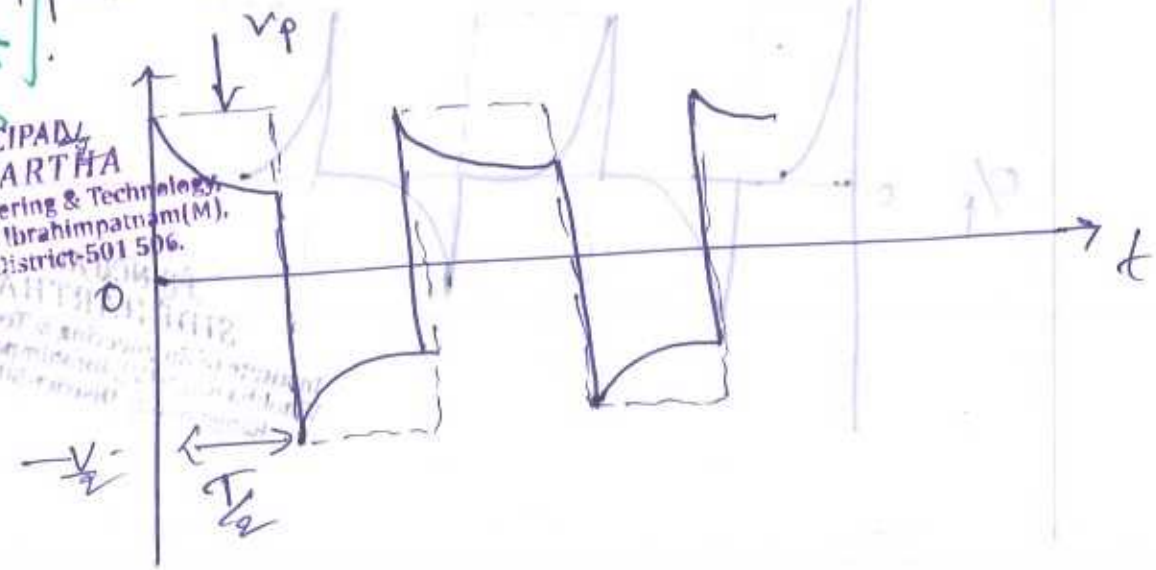
SIDDHARTHA
Institute of Engineering & Technology,
Vinobha Nagar(V), Ibrahimpatnam(M),
Ranga Reddy District-501 506.

At $t = T/2$ the input voltage drops from $+\frac{V}{2}$ to $-\frac{V}{2}$ abruptly, Hence the O/p voltage must also drops by the same amount $V_i < V$, $V_o = -V$ at $t = T/2$ The voltage $-V$ rapidly and exponentially towards zero.

Case(ii) Let $RC \gg T$ i.e $\tau/T \gg 1$

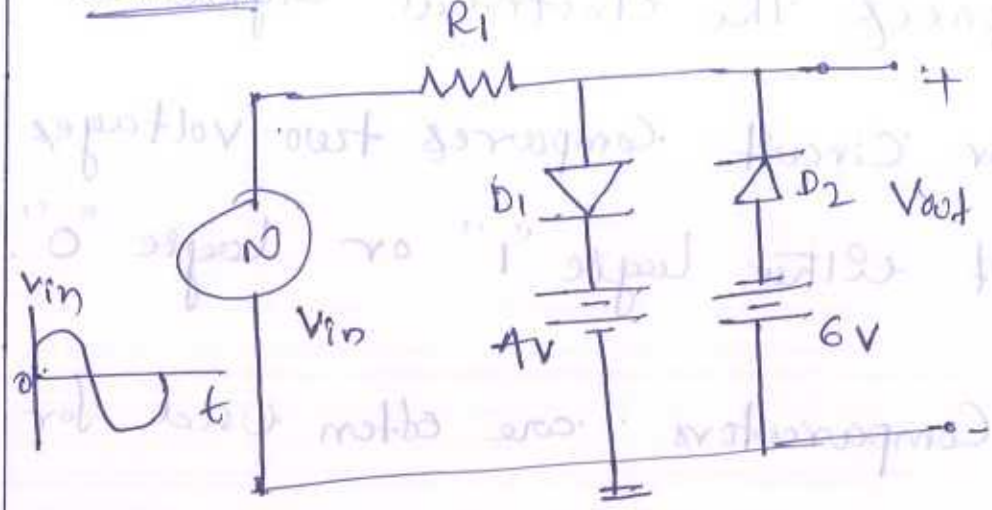
If the time constant is quite large the exponential decay of the output voltage is slower as seen already, This results in a tilt at the top of the O/p wave and under shoot at the bottom, as is obvious from the output wave form.

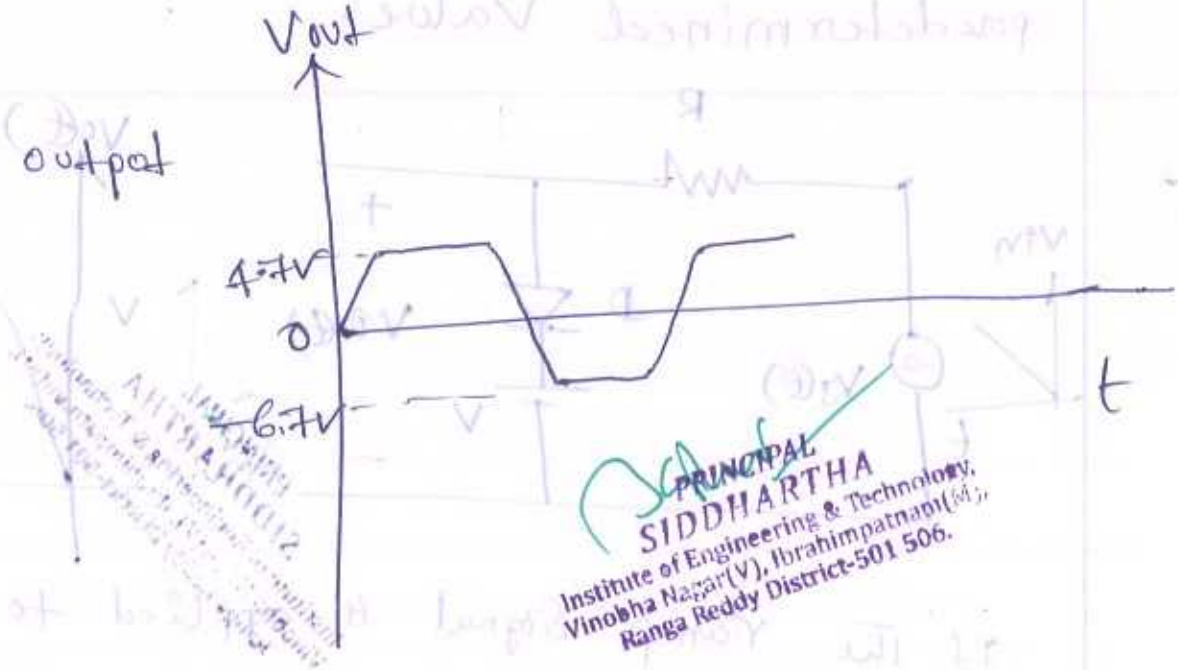


4 a) Explain the operation of two level slicer?

A Circuit which slice the two levels either positive and Negative peaks.

Circuit:

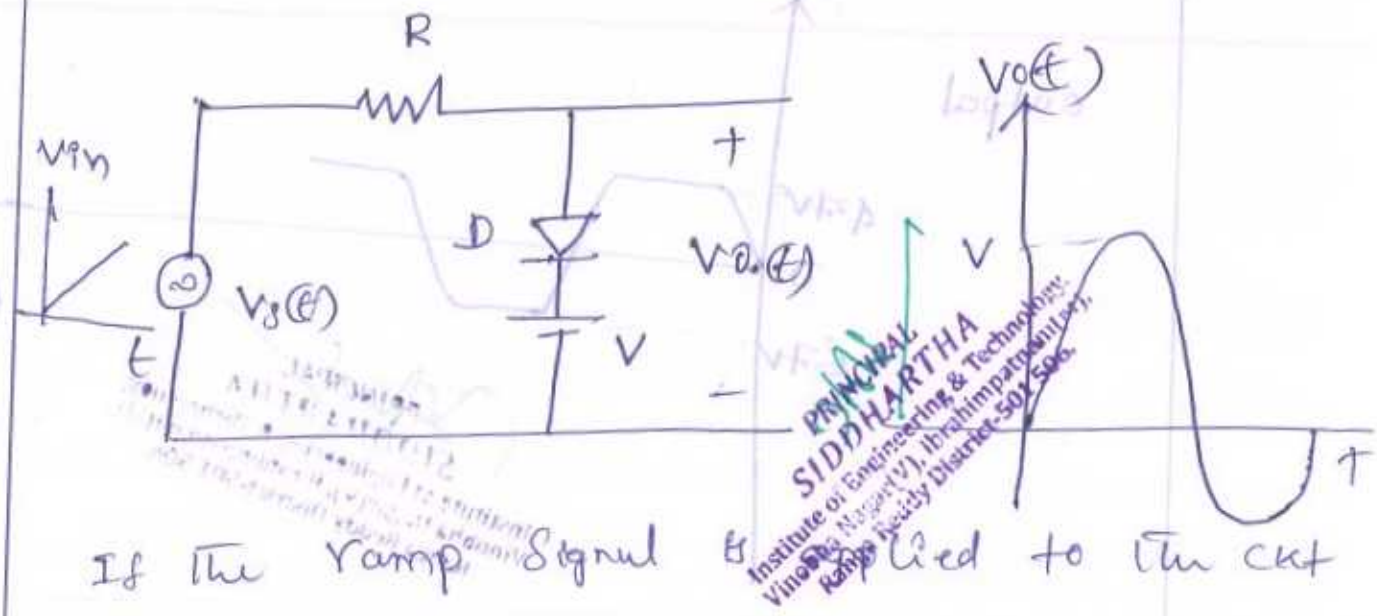




4 b) What is ment by Comparator? Explain The Applications of voltage Comparators.

Comparator is an electronic Circuit which Compares the electrical Signal. or A Comparator Circuit Compares two voltages and the output either Logic "1" or Logic "0".

Comparators are often used for check Whether an Input has reached some predetermined value.

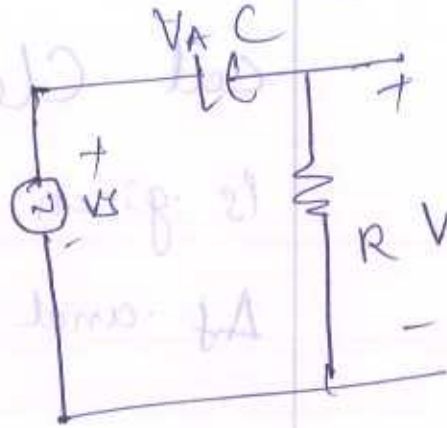


If the ramp Signal is applied to the ckt the output is Constant V_R voltage until the ramp Signal reduces a value equal to V_R the nal. Conducts and the I/p appear at the output.

5a) State and prove Sampling Theorem 2.5M

In steady state, the Area A_f under the output voltage waveform in the forward direction when the diode conducts is related to the area A_r in the reverse biased direction. When the diode does not conduct by the relationship

$$\frac{A_f}{A_r} = \frac{R_f}{R_r}$$



$V_f(t)$ F.B output voltage

$$i_f(t) = V_f(t)/R_f$$

$$\int_0^T i_f(t)\,dt = \frac{1}{R_f}\int_0^T V_f\,dt = \frac{A_f}{R_f}$$

$V_r(t)$ is the output voltage in reverse direction, then the current which discharges

$$i_r(t) = V_r(t)/R$$

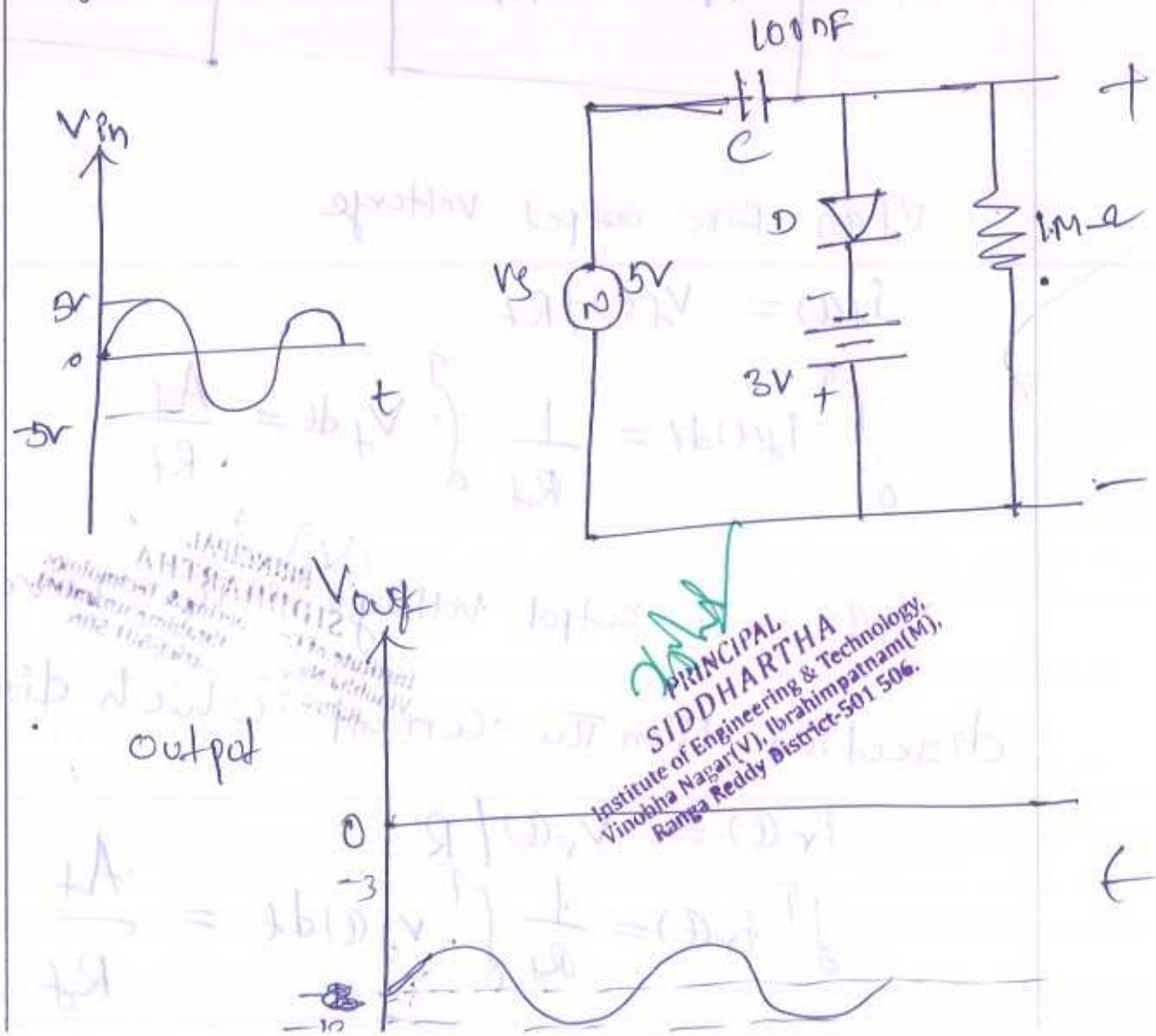
$$\int_0^T i_r(t) = \frac{1}{R_f}\int_0^T v_f(t)\,dt = \frac{A_f}{R_f}$$

$$\int_{T_1}^{T_1+T_2} i_1(t)\,dt = \frac{1}{R}\int_{T_1}^{T_1+T_2} V_r(t)\,dt = \frac{A_r}{R}$$

$$\therefore \boxed{\frac{A_f}{A_r} = \frac{R_f}{R_r}}$$

---

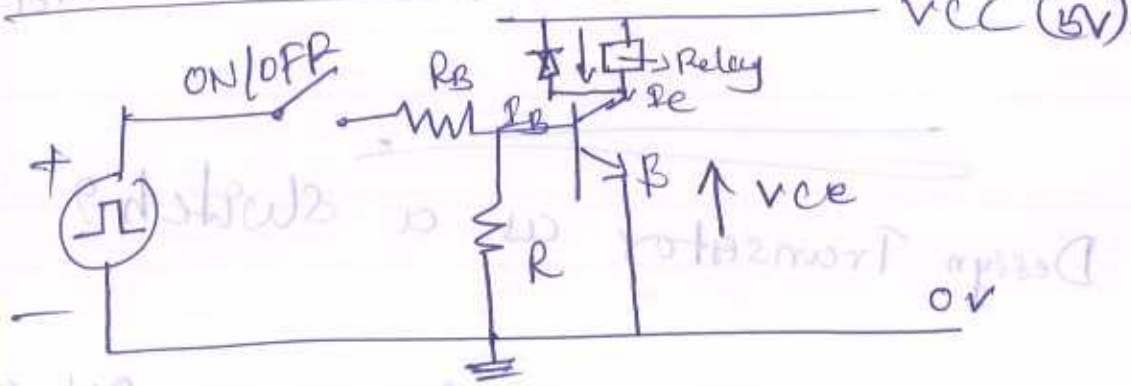
5 b) Draw the output wave form of practical Clamping Circuit when a Square wave is given as input. Derive the relation B/w A_f and A_r in this case



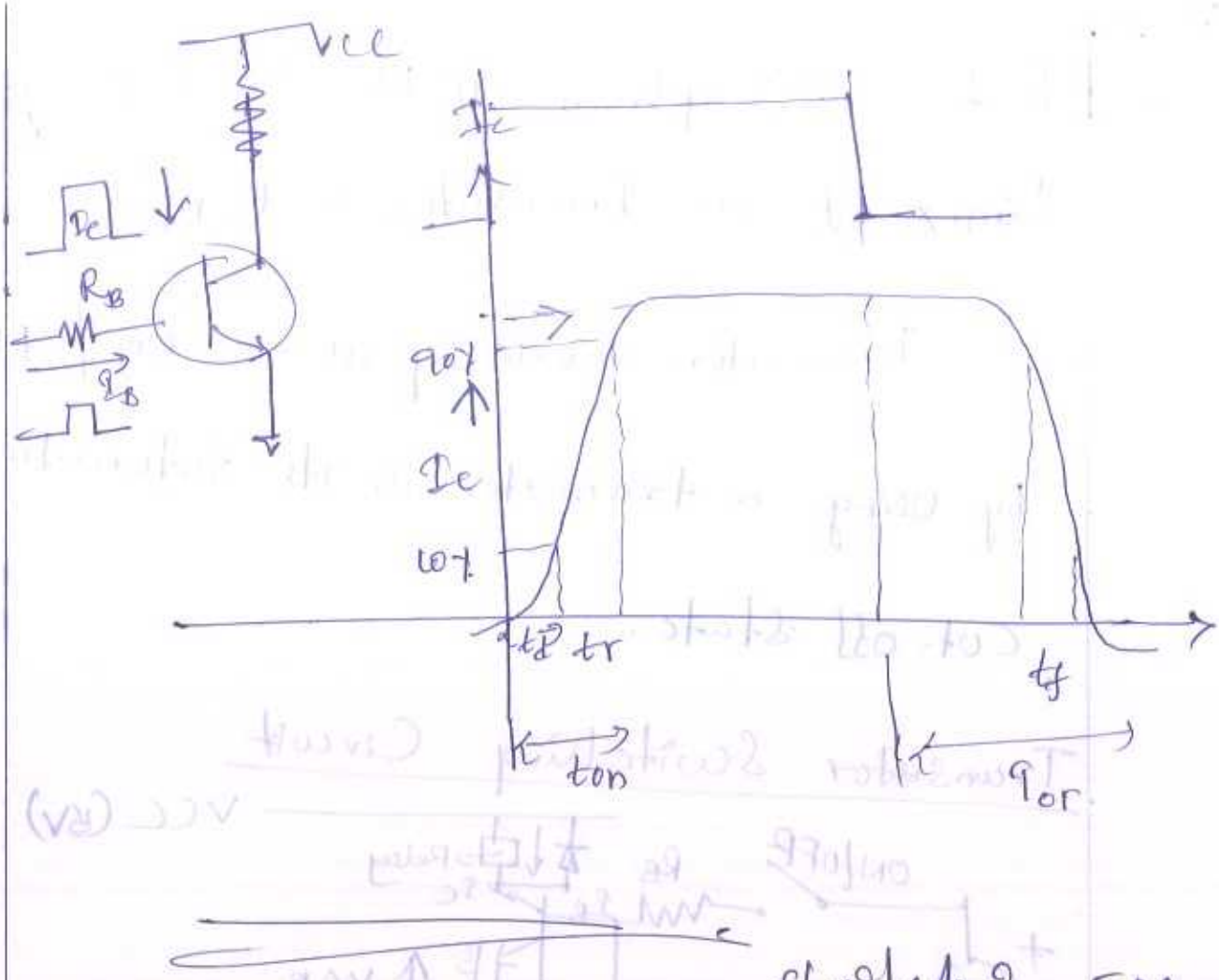
6. Let and explain all the Switching times of a Transistor? [10M]

Transistor working as a "ON"/OFF Switch by using a transistor in its saturation or cut-off state.

Transistor Switching Circuit



The difference in time this transistor is that to operate the transistor as switch either fully OFF or fully ON. Used to switch and control lamps, relays or even motors



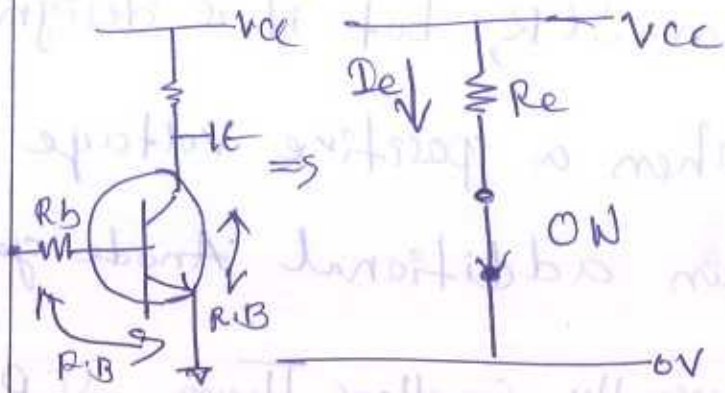
7(a) Design Transistor as a switch? 5M

Transistor working as a ON and OFF switch. Transistor working as "ON" switch in Saturation region, OFF switch in Cutoff region operation.

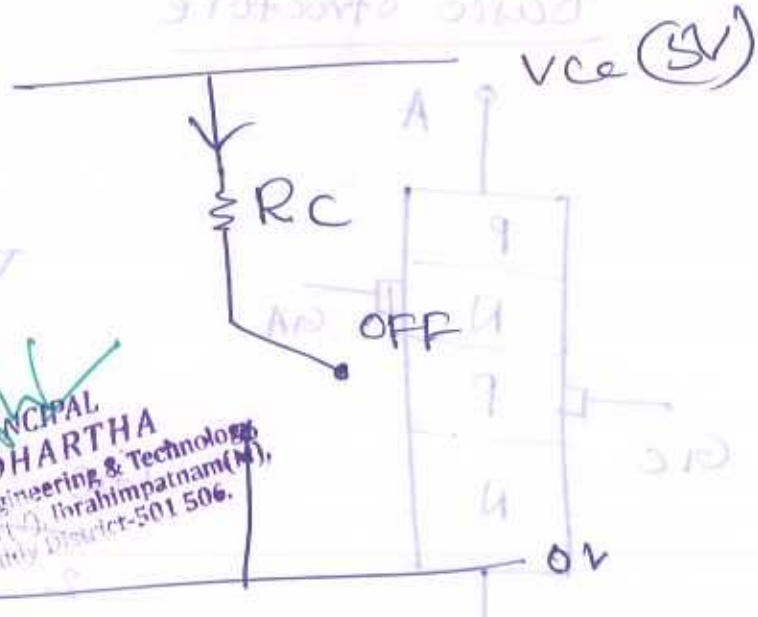
Apply EB Junction R.B CB Junction

R.B Transistor working as an Amplifi

→ And EB and EB Both or F.B transistor operating in Saturation region working as ON switch



→ And EB and EB Both Junctions are in R.B transistor working as a OFF Switch



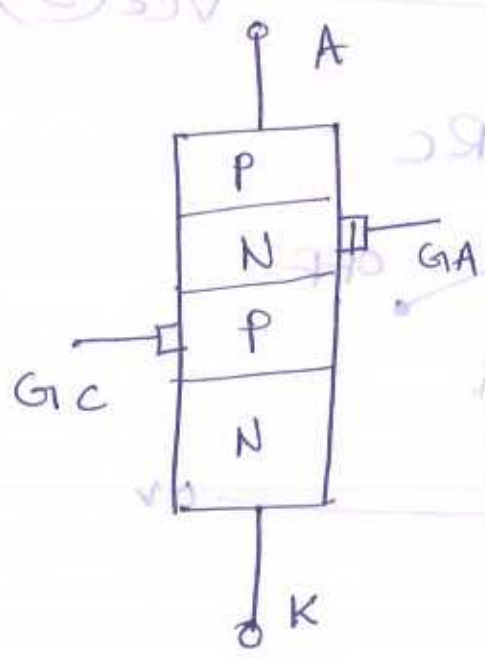
7(b) Explain in detail about Silicon Controlled Switch Circuits?

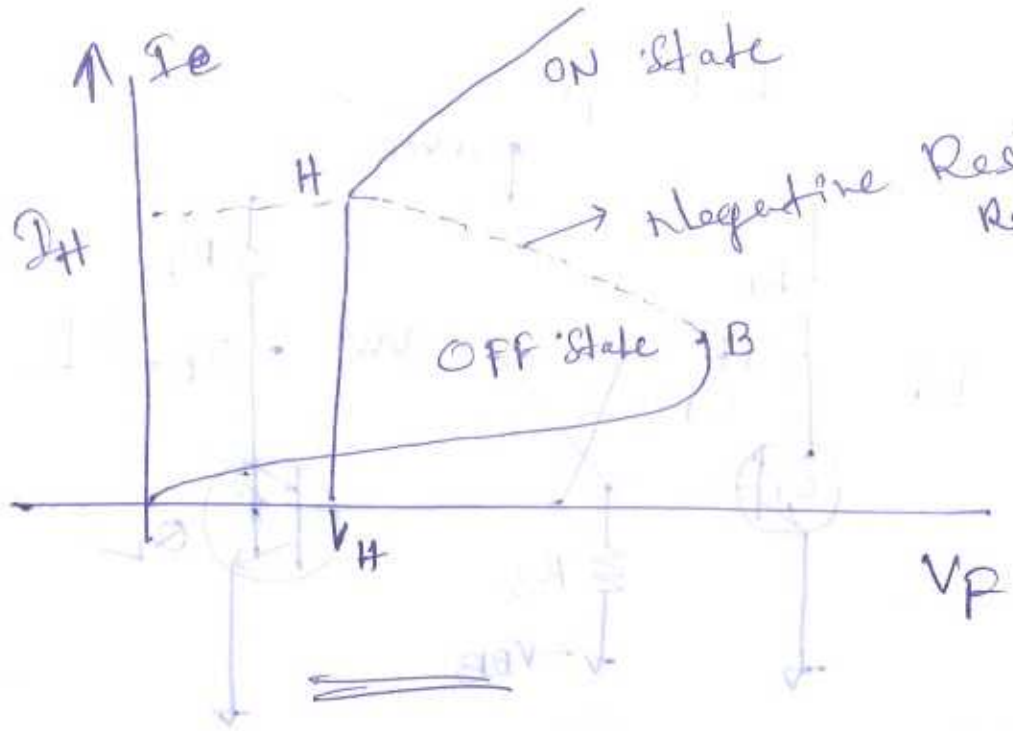
It is an power Semiconductor device Similar to an SCR, but it is designed to turn off when a positive voltage pulse is applied to an additional Anode gate terminal

It is physically smaller than SCR, lower leakage and holding current than SCR

It requires smaller triggering signals.

Basic structure





V_F increases, the current initially is extremely small and increases extremely slowly upto point A on the characteristic. Beyond point A current increases rapidly. At voltage corresponds to point B, device switch ON

8 a) With the help of neat circuit Diagram and waveforms, explain the principle of operation of Collector Coupled monostable multivibrator?

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SIDDHARTHA
Institute of Engineering & Technology,
Vinobha Nagar(V), Ibrahimpatnam(M),
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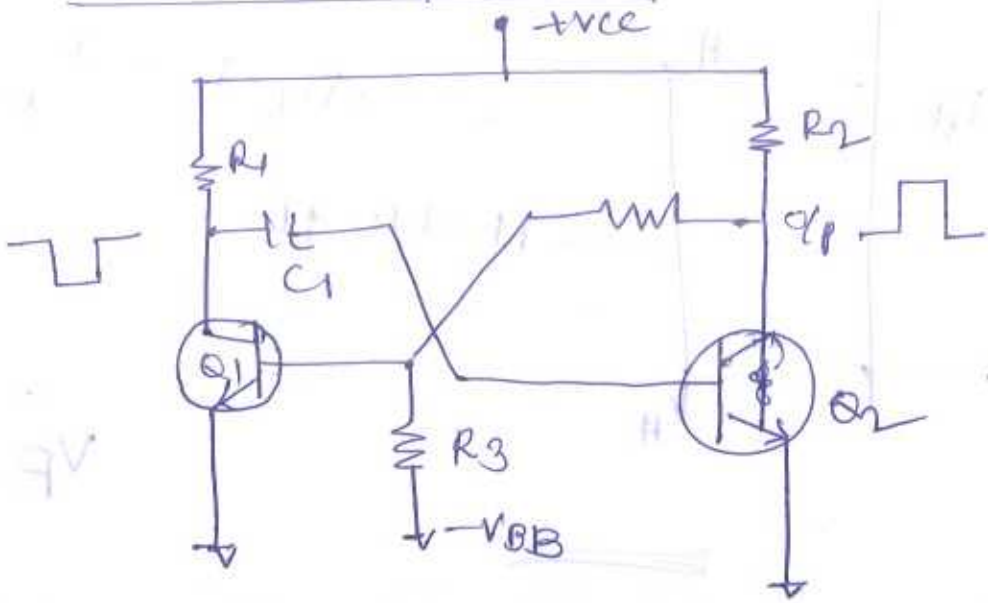
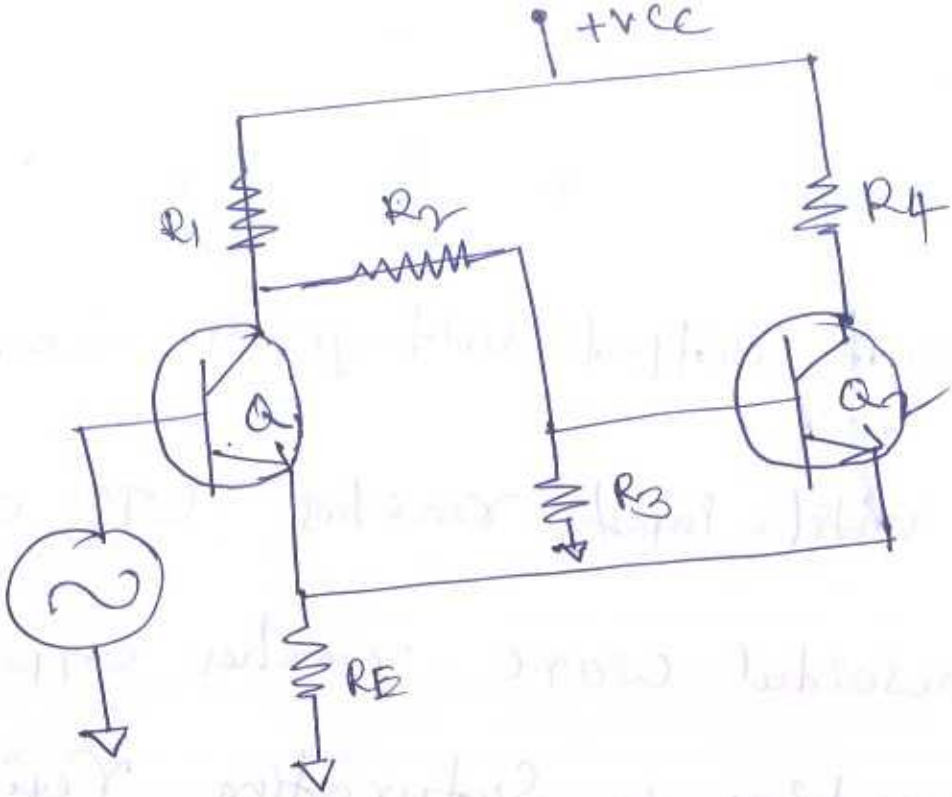
Circuit Diagram



→ Monostable multivibrator has only one stable state, it is stable at logic "0" or logic "1". It has one quasi stat

→ When the circuit is switched ON, transistor Q_1 will be OFF and Q_2 ON. This is the stable state. This decreases the collector voltage, which turns OFF the transistor Q_2. Thus capacitor C_1 starts discharging

3 b)
2. Schmitt trigger working using transistor 5M



→ Schmitt trigger is an electronic device it converts Sinewave to Squarewave.

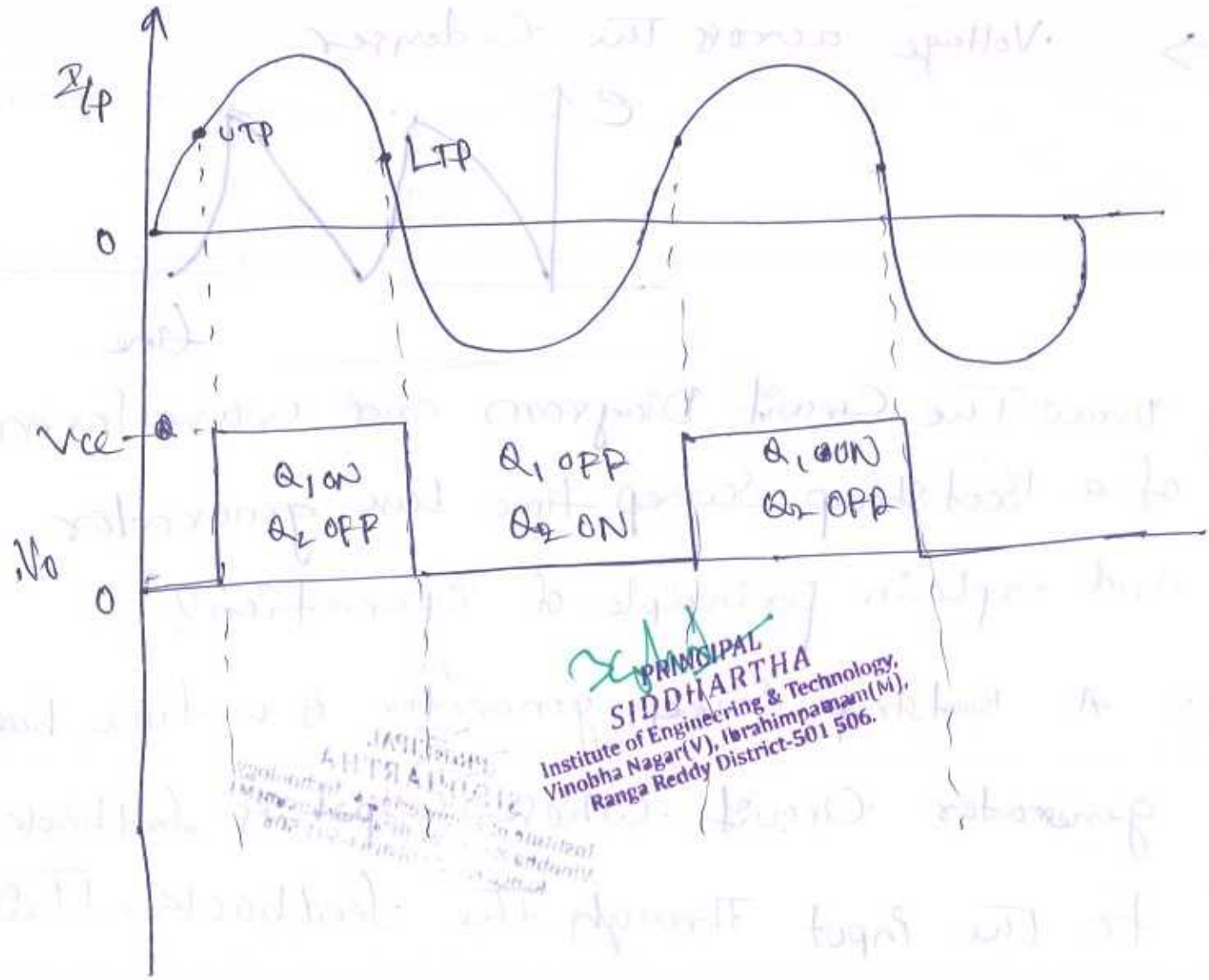
→ Schmitt trigger operation is similar to Bistable multivibrator, It is operating at two triggering points UTP, LTP.

→ Apply the Vcc, Input Sinusoidal Signal to the Schmitt trigger Circuit current

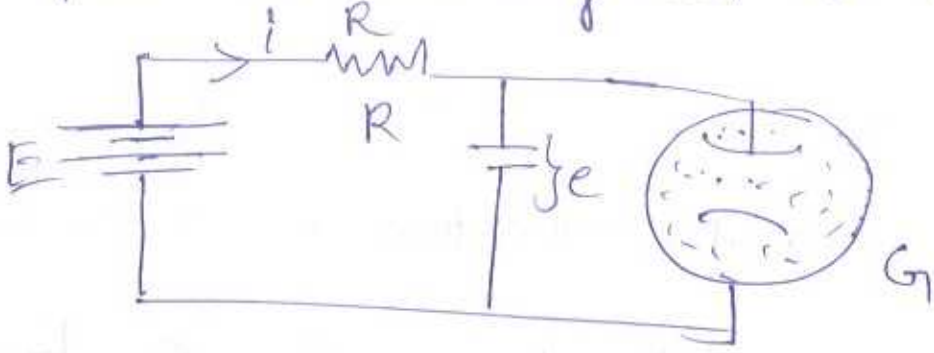
passes Through $R_1 \rightarrow R_2 \rightarrow$ Base of Q_2 transistor causes Q_2 transistor turn "ON" it is operating in Saturation Region, acts as Short Circuit output voltage is ~~Zero~~.

→ Q_1 OFF until input reaches UTP, once input Sinusoidal wave reaches UTP Q_1 ON it is operating in Saturation Region acting as Short Circuit output voltage is Zero across collector terminal. This low voltage given to Base of Q_2 transistor to make turn OFF. so, it is Operating in Cutoff Region, act as o.c output voltage is maximum.

→ The input Sinosoidal Signal reaches LTP "Q1 OFF operating en Cutoff region, output Voltage across Collector is maximum; the Voltage given to base of "Q2 transistor it's turn "ON" operating en Saturation region, output voltage is minimum.

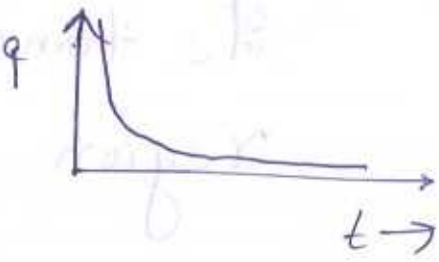


9a) Draw a Simple Current Sweep Circuit and explain its working with the help of diagram?



→ current rate depends on the R and c value

→ Current flow into the Condenser

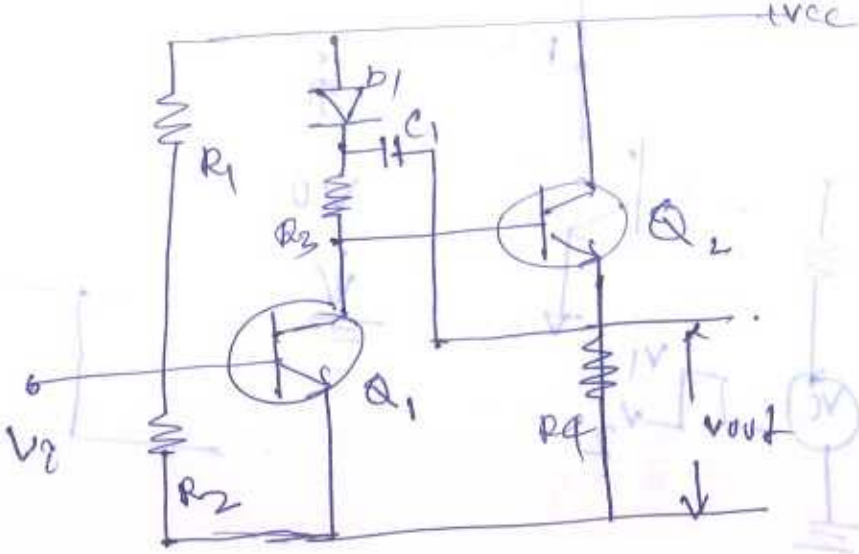


→ Voltage across the Condenser

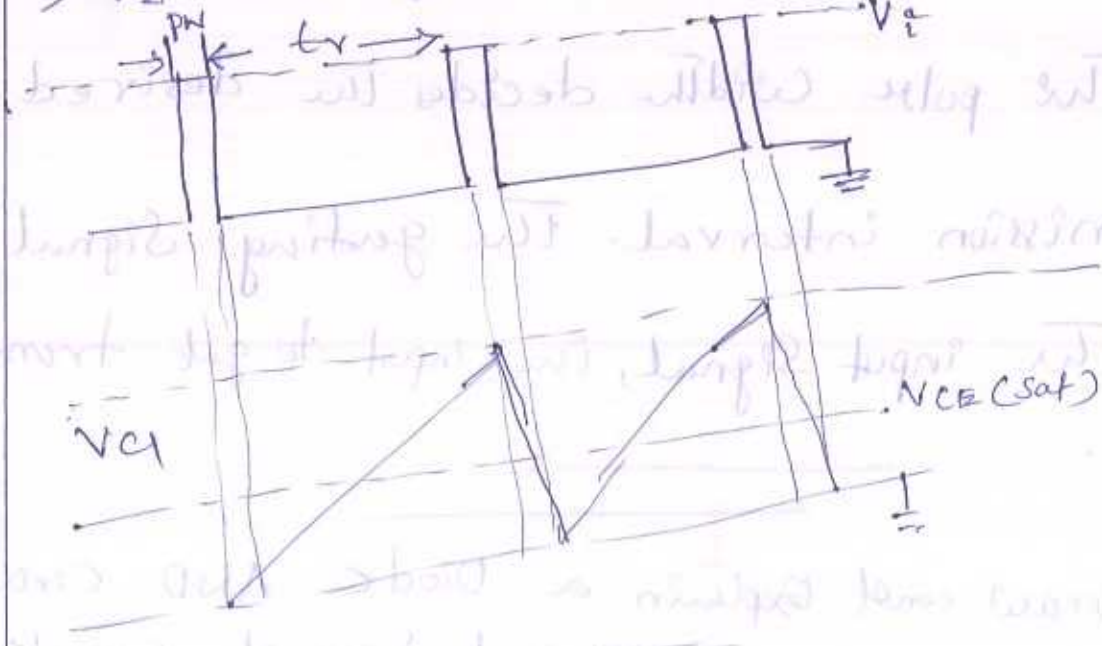
9b) Draw the Circuit Diagram and waveforms of a Bootstrap Sweep time base generator and explain principle of operation?

→ A Bootstrap Sweep generator is a time base generator circuit which uses feedback to the input through the feedback. This

This process of bootstrapping is used to achieve Constant Charging current.



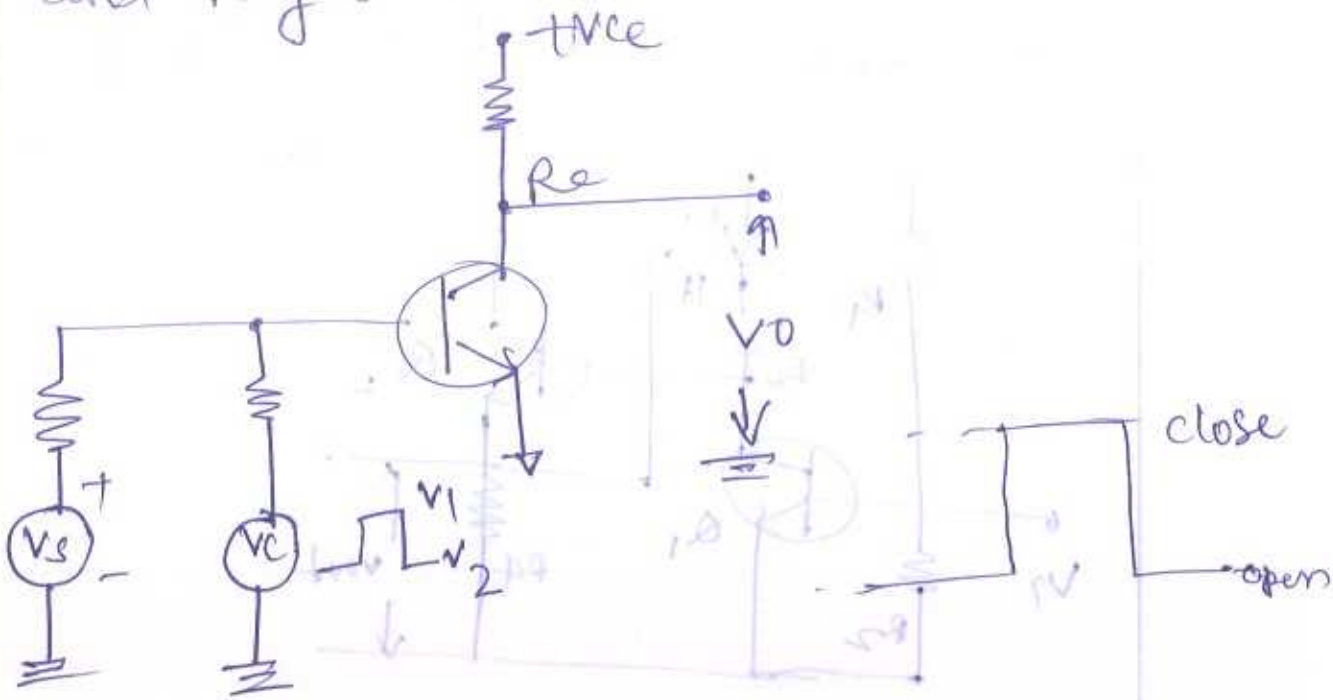
→ It act as a emitter follower



10 a) With with the help of neat Diagram Explain the working of Bidirectional gates using transistor

Bidirectional gate transmits two polarities of the signal either positive

and Negative.



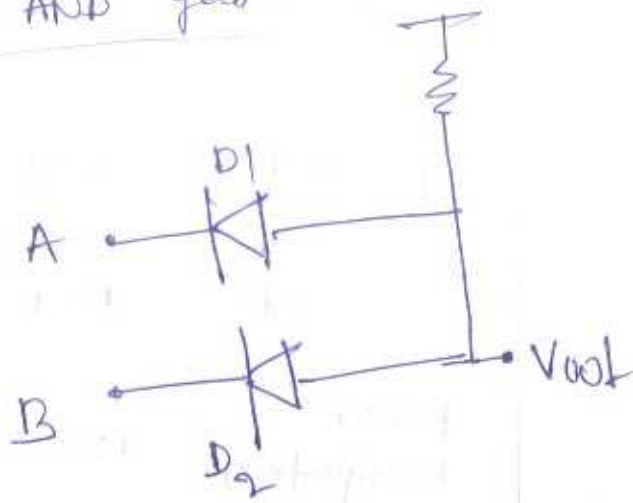
→ A control input is applied at V_1, V_2 levels. The pulse width decides the desired transmission interval. The gating signal allows the input signal, the input to get transmitted.

10(b) Draw and Explain a Diode AND Circuit for negative logic and how it works. How can OR gate Circuit act as a Buffer?

→ Negative polarity means signal and output polarity is indicated by a bubble or triangle.

Negative logic AND gate

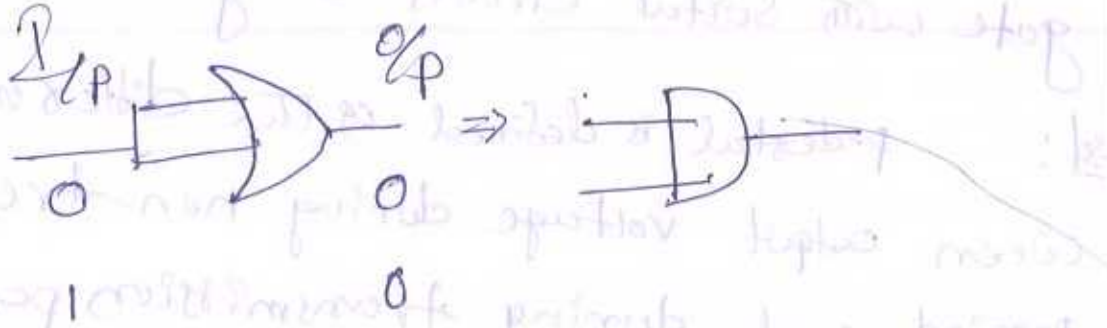
A	B	A·B
1	1	1
1	0	0
0	1	0
0	0	0



→ A Buffer has only a single input and a single output with behaviour that is the opposite of an NOT gate.

→

I/P	output
L	L
H	H

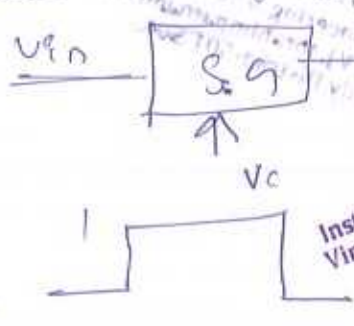


11a) Compare various Logic families

parameter	RTL	IIL	DTL	TTL	ECL	CMOS
Basic gate	NOR	NOR	NAND	NAND	OR NOR	NOR NAND
power Dissipation (mW)	12.	6mW	8-12	10	40-55	1.01
Fanout	5	Dependson Injected current	8	10	25	20
Noise Immunity	Normal	poor	Good	V.good	poor	V. Good
Delay	12	25-250	30	10	2	70
Speed	144	<1	300	101	100	0.7

11b) Explain how to cancel a pedestal in sampling gate with suitable Circuit Diagram?

Sol: pedestal is defined as the difference between output voltage during non-transmission period and during transmission period with Zero Signal.

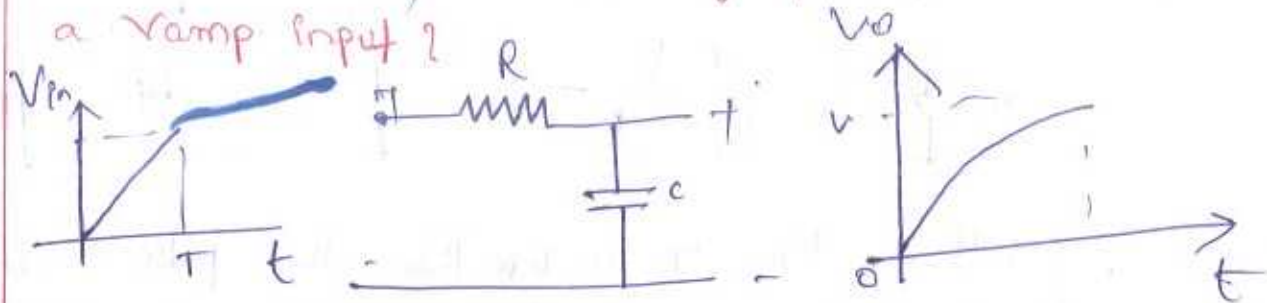


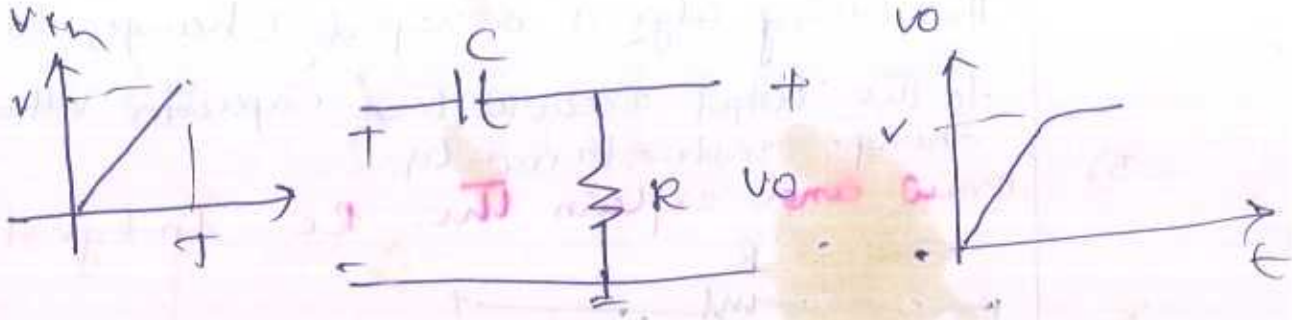
$V_o = V_S$ during Transmission period

0 during non-Transmission period.

UNIT - I

1) Obtain The Responce of high pass RC Circuit for a Ramp Input ?





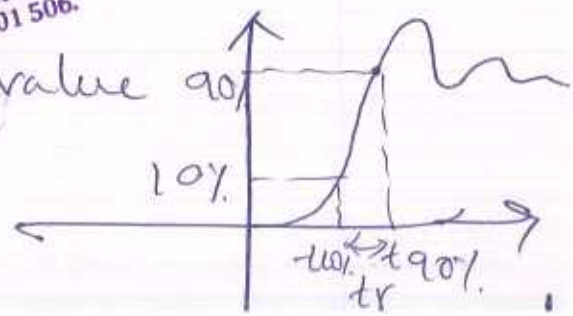
2) Define The % Tilt for a RC Circuit ?

% Tilt is defined as decay in the amplitude of the output voltage wave due to the input voltage maintaining level.

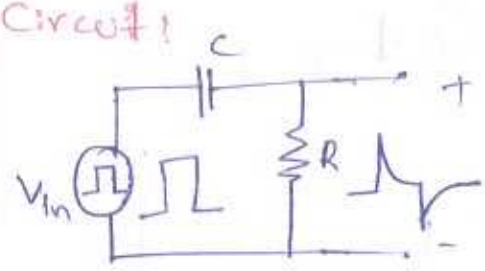
$$\% \text{ Tilt} = \frac{V_1 - V_1'}{(V/2)} \times 100$$

3) Define Rise time (t_r) ?

A voltage or current pulse rise from 10% to 90% of its steady value



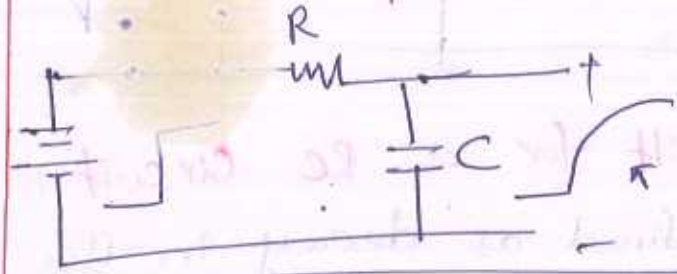
4) Draw and briefly explain the RC differentiator circuit?



$$V_o = RC \frac{dV_{in}}{dt}$$

When time τ is less than the pulse width ($\tau << t_w$) the falling edge is a rapid change, so it is passed to the output because the capacitor voltage cannot change instantaneously.

5) Draw and explain the RC Integrator circuit?



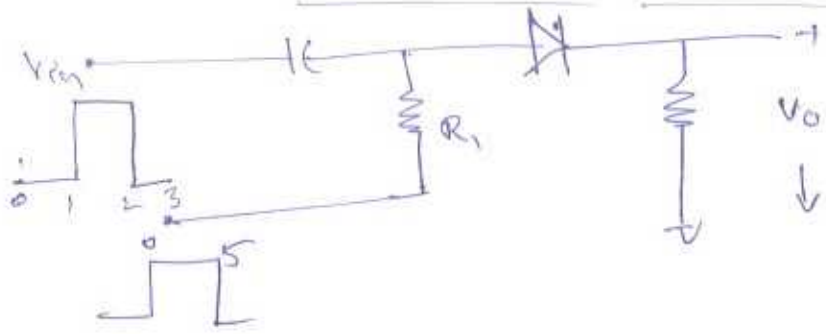
The output is an exponentially rising curve ($\tau >> \frac{1}{t_w}$)

$$V_o = \frac{1}{RC} \int V_{in} dt$$

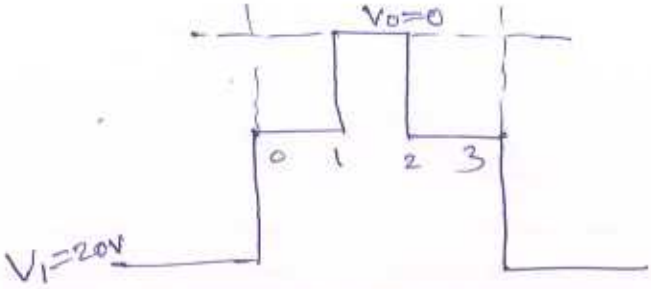
6) What is ment by Linear network?

A Linear network is one which consists of R, L, C elements, whose parameters does not change with current or voltage.

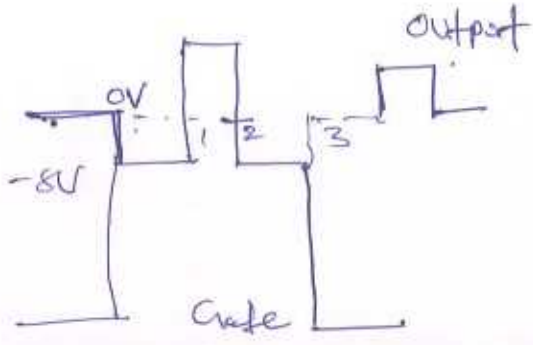
Unidirectional Sampling gate



output

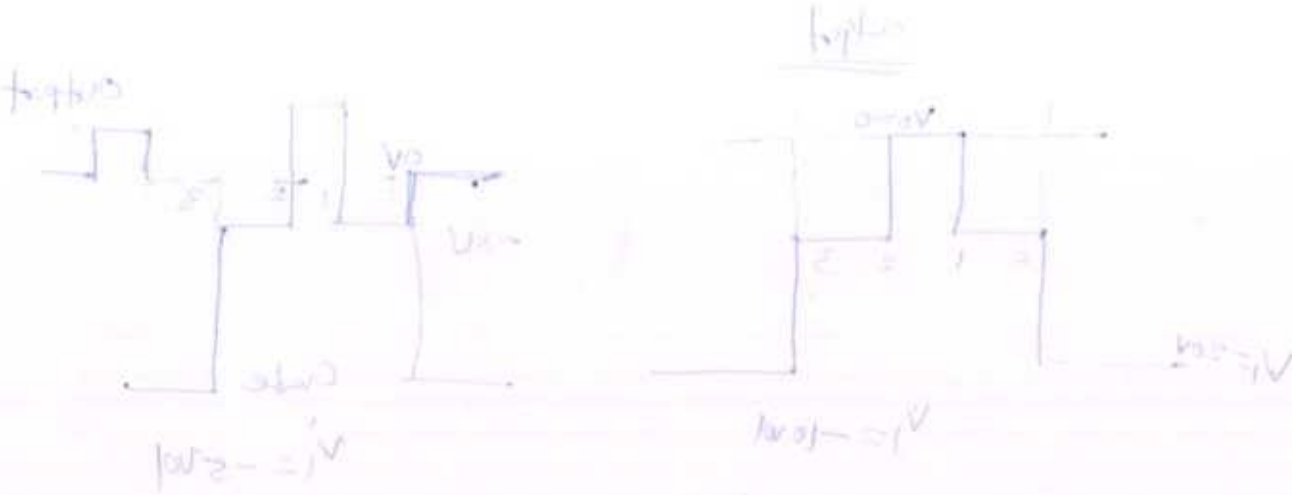


$V_1 = -10V$



$V_1 = -5V$

PRINCIPAL
SIDDHARTHA
Institute of Engineering & Technology,
Vinobha Nagar(V), Ibrahimpatnam(M),
Ranga Reddy District-501 506.



7) Why Rc Circuits are commonly Used Compare to RL Circuits?

RC and RL Circuits are used to provide filtering, Wavershaping, and timing, the capacitor is most commonly used. Capacitors are smaller and more economical than inductors.

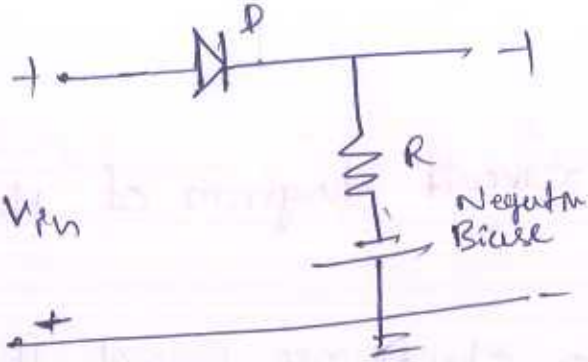
PRINCIPAL
SIDDHARTHA
Institute of Engineering & Technology,
Vinobha Nagar(V), Ibrahimpatnam(M),
Ranga Reddy District-501 506.

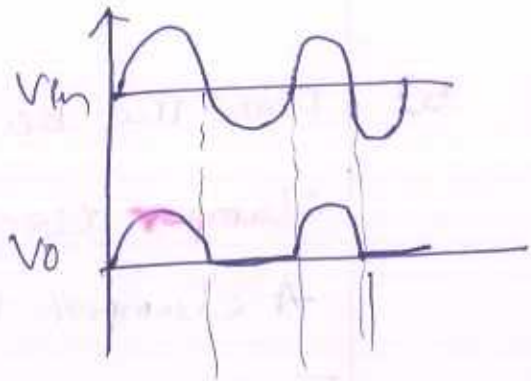
UNIT- II

1 Write the Applications of voltage Comparator?

Zero crossing detectors, switching power Regulator peak detectors. Motors.

2) Draw the Negative Biased Negative Clipper circuit?



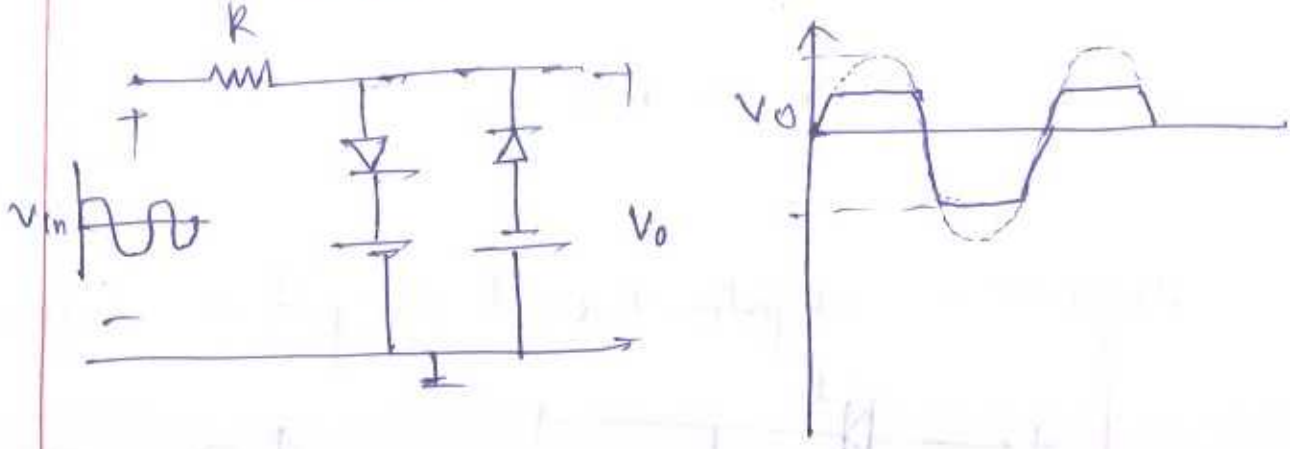


3) What is meant by clipping in wave shaping?

A clipper is a device which removes, limits or prevents some portion of the input wave form.

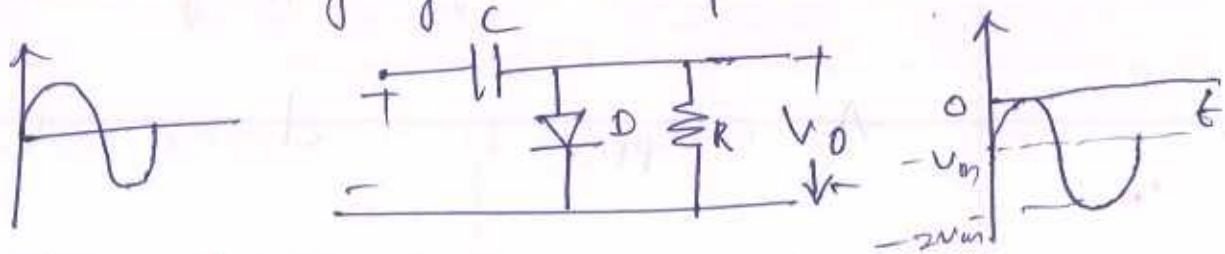
PRINCIPAL
SIDDHARTHA
Institute of Engineering & Technology,
Vinobha Nagar(V), Ibrahimpatnam(M),
Ranga Reddy District-501 506.

4. Explain clipping at two independent levels with circuit?



5) Draw the basic circuit diagram of Negative peak clamper circuit.

A clamper is an electronic circuit that changes the DC level of a signal to the desired level without changing the shape of the input signal



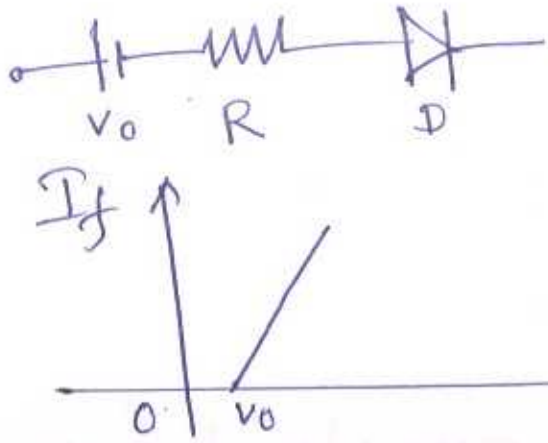
6) Distinguish between comparators and clipping circuits.

→ Comparator compares the two inputs and produces the one output.

→ Clipping circuit add some DC level to the input wave form.

UNIT – III

1. Draw the piecewise linear Diode characteristics?



2. When transistor acts as a switch?

→ Transistor is working as an "ON" switch in Saturation Region operation

→ Transistor is acting as "OFF" switch in cut-off Region operation.

3. Explain the variation of ~~temparature~~ Saturation parameters of ~~transistor~~ with Temparature?

4. How does diode acts as a switch?

→ Diode is acts as "ON" switch in Forward biase Condition

→ Diode is acts as OFF switch in Revese biase Condition

5. What do you mean by turn ON time of a transistor?

→ Turn ON Time of a transist is time taking to turn-on the transistor

UNIT-IV

1. Define Multivibrator?

→ Multivibrator is an electronic circuit which is used to design two states devices

2. Compare different multivibrators?

1) Astable multivibrator having two unstable states
2) Mono stable Multivibrator having one stable, one unstable states
3) Bi-stable Multivibrator having two stable states.

3. Write a basic principle of time base generator?

→ Time base generator generates time base signal which Amplitude is linearly varying with respect to time.

4. Write the Methods of Generating Time Base waveform.

→ Current time base generator
→ Voltage time base generator
→ Miller sweep time base generator
→ Boot strap sweep generator.

5. Write the difference between current time base generator and voltage time base generator

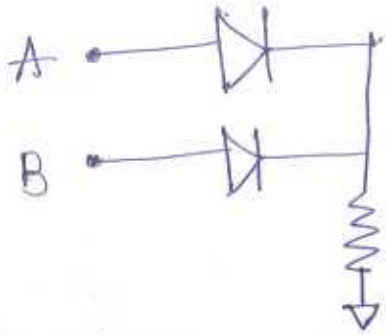
→ Current time base generator generates current Time base Signal

→ Voltage time base generator generator voltage time base Signal.

6 Explain the frequency division in the Sweep ckt?

UNIT – V

1. Draw the OR gate using Diode?



2. Why totem pole is used in DTL?

→ Totem pole Circuit is used to reduce the propagation delay in Logic Circuits.

3. How does Sampling gate is different from Logic gate

→ Sampling gate is produce the replica of input waveform, it accepts only one input produce one output, it does not perform Logical operation.

→ Logic gate perform Logical operation, it accepts number of inputs, and produce one output

4) Compare MOS and CMOS families.

→ MOS family is used to fabricate IC's, having less speed, Less fan-out

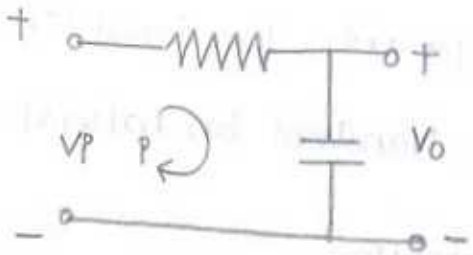
→ CMOS having combination of N-MOS, P-MOS, having Low power consumption, high Fan-out.

5. Compare DTL, TTL, CMOS ?

UNIT- I

Linear Wave shaping

1.1 Low pass RC circuit :-



Let V_i denote the input voltage, and V_o the output voltage. It may be observed that this ckt is the same for high pass RC circuit studied earlier. so far as the circuit configuration is concerned. however there is one basic difference, where as - in the high pass circuit the output is taken across the resistor in the circuit under consideration the o/p is taken across the capacitor.

Since the reactance of a capacitor decreases with increase of frequency and vice versa it can be seen that the capacitor offers much large impedance to the low frequency components pass out easily to the o/p without any appreciable attenuation. The circuit is therfore called L.P RC ckt.

Let 'i' denote the ckt current.

we have $V_i = V_o + V_R$ applying KVL to the closed loop

$V_R = i R$ the voltage drop across R, and

$V_o = V_c$ the voltage drop across the capacitor.

$$i = C \frac{dV_c}{dt} = C \frac{dV_o}{dt}.$$

$$\therefore V_i = V_o + RC \frac{dV_o}{dt}$$

dividing throughout by RC we get

$$\boxed{\frac{V_1}{RC} - \left(\frac{1}{RC}\right) V_o + \frac{dV_o}{dt}}$$

This is the basic relationship connecting the o/p with the i/p of a low-pass RC ckt.

In this expression $\left(\frac{1}{RC}\right) V_o$ represents the forced (or) steady state response & $\frac{dV_o}{dt}$ represents the transient (or) natural response.

1.2 Low pass RC circuit as Integrator :-

We studied that for a low pass RC ckt.

$$\left(\frac{1}{RC}\right) V_o + \frac{dV_o}{dt} = \frac{V_1}{RC}.$$

RC is the time-constant of the circuit

let it be assumed that $RC >> T$ the periodic time of the i/p signal V_i

For a large time constant, it is evident that the output taken a fairly long time to come to steady state as such the transient response is very important and the steady state response becomes insignificant and hence can be ignored.

putting $\left(\frac{1}{RC}\right) V_o = 0$ we have :

$$\frac{dV_o}{dt} = \left(\frac{1}{RC}\right) V_i$$

Integrating b.s.t wrt 't' we get

$$V_o = \int \frac{1}{RC} V_i \, dt$$

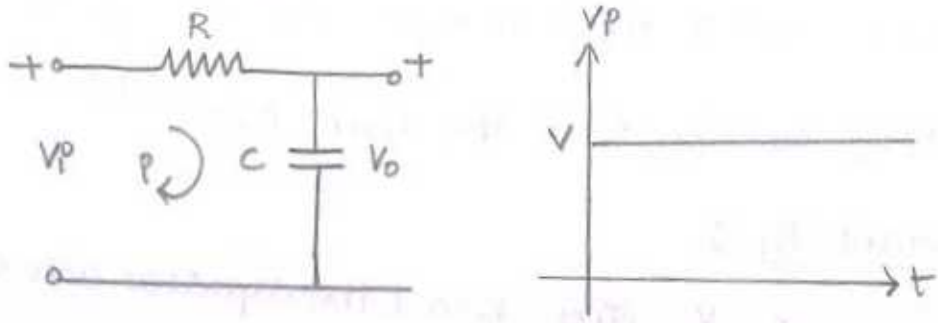
(or) $$\boxed{V_o = \frac{1}{RC} \int V_i \, dt}$$

Since R and C are fixed in magnitude, we have.

$$V_o \propto \int V_i \, dt$$

that is the o/p is proportional to the time integral of the input for this reason, the low pass RC ckt with $RC >> T$, is called RC "Rc integrator"

1.3 Response of low pass RC circuit to step voltage input :-



$V_i = 0$ for $t < 0$
$= V$ for $t > 0$.

let the forcing function be a step voltage V. Due to the applied voltage, a current 'i' results. It is evident that at $t = (0-)$

$V_i = 0$ and $V_o = 0$.

At $t = (0+)$ also $V_i = 0$ & $V_o = 0$.

For $t > 0$, since the capacitor initially acts as a short circuit, a current flows & the capacitor charges. As charging progresses, more and more voltage developes across C, and the current 'i' progressively diminishes, and eventually it becomes zero.

It shows that the output characteristics is a rising exponential.

Applying KVL to the RC circuit, we have for $t > 0$ $V_i = V_R + V_o$

$$V_R = iR \quad \text{and} \quad V_o = V_c = \frac{1}{C}\int i\,dt$$

$$\therefore V_i = iR + \frac{1}{C}\int i\,dt$$

But $V_i = V$ for all $t > 0$.

$$\therefore iR + \frac{1}{C}\int i\,dt = V$$

diff wrt 't' we get

$$R\frac{di}{dt} + \frac{1}{C} i = \frac{dV}{dt} = 0 \text{ , since } V \text{ is of constant magnitude}$$

$$\text{(or)} \quad \frac{di}{dt} + \left(\frac{1}{RC}\right) i = 0$$

The solution of this diff eqn of the form i = complimentary function + particular integral. The particular integral is zero, since it represents the steady state response and we have $i = 0$ at $t = \infty$

The complimentary function is of the form $K_1 = e^{-t/RC}$.

To find the constant K_1 :-

at $t = 0$, we have $i = \frac{V}{R}$ since $V_c = 0$ (the capacitor acts as S.C and the voltage across it is zero.

$$\therefore \frac{V}{R} = K_1 e^0 \text{ , putting } t = 0.$$

$$\therefore K_1 = \frac{V}{R}.$$

It is assumed that the initial capacitor voltage is zero.

$$\therefore \boxed{i = \frac{V}{R} e^{-t/RC}}$$

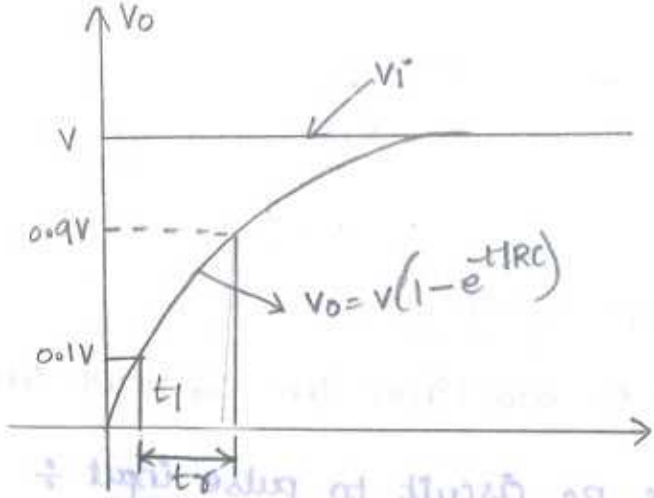
O/P voltage $V_0 = V_c = V_i - iR$.

$$\text{(or)} \quad V_0 = V - \left(\frac{V}{R} e^{-t/RC}\right) R$$

$$= V - Ve^{-t/RC}.$$

$$\boxed{\text{(or)} \quad V_0 = V\left[1 - e^{-t/RC}\right]}$$

The graph of V_o Vs t is as shown in fig.



t_r = Rise time
$= t_2 - t_1$.

1.3.1 Rise time (t_r) :

Referring to fig it is seen that the o/p voltage V_o increases exponentially and after a pretty long time (theoretically at $t = \infty$) attains the steady value V. The time required for the voltage to rise from 10% to 90% of the final steady value is termed as rise time. It is denoted as t_r.

It can be shown that $t_r = 2.2\,RC$.

Proof :

At $t = t_1$, $V_o = 0.1V$

$\therefore 0.1V = V(1 - e^{-t_1/RC})$

(or) $e^{-t_1/RC} = 1 - 0.1 = 0.9$

(or) $e^{-t_1/RC} = \log_e 0.9$

$\therefore t_1 = -RC \log_e 0.9$ ——— (1)

At $t = t_2$ $V_o = 0.9V$.

$\therefore 0.9V = V(1 - e^{-t_2/RC})$

(or) $e^{-t_2/RC} = 1 - 0.9 = 0.1$

$$(or) -t_2/RC = \log_e 0.1$$

$$(or)\ t_2 = -RC \log_e 0.1 \quad \text{——— (2)}$$

we have rise time $\boxed{t_r = t_2 - t_1}$

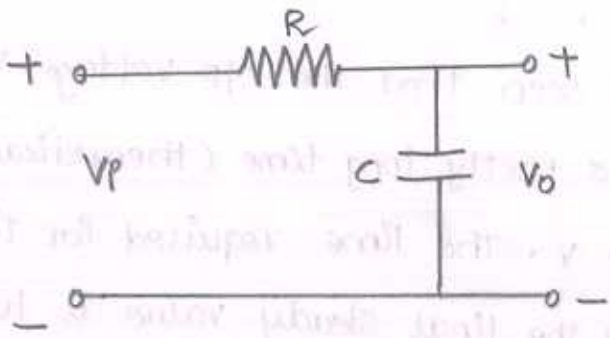
$$= -RC(\log_e 0.1 + \log_e 0.9)$$

$$= 2.2RC.$$

$$\boxed{\therefore t_r = 2.2RC}$$

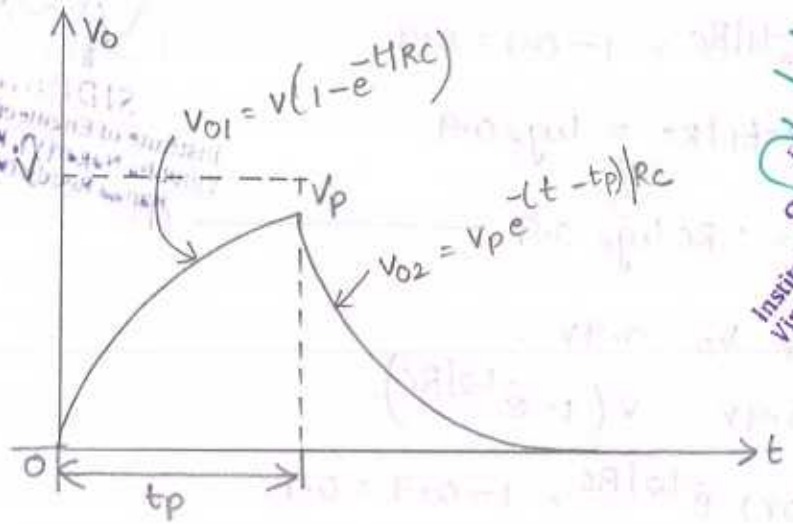
Hence the rise time is 2.2 times the constant time.

1.4 Response of low-pass RC circuit to pulse input :



let a pulse voltage be applied to a low pass RC circuit

It is evident that for $t>0$ but t_p the pulse width, the pulse voltage is exactly alike a step voltage and hence the o/p voltage increases exponentially from 0 to V_p at the end of the pulse. At $t=t_p$ the i/p voltage drops to zero & hence the o/p decreases exponentially and becomes zero at $t=\infty$ The o/p curve is as shown in fig.



while the o/p voltage is exponentially increasing, we have

$V_{o1} = V(1-e^{-t/RC})$ where V = Amp of i/p pulse.

let $V_{o1} = V_p$ at the end of the pulse at $t = t_p$

obviously $V_p < V$

For $t > t_p$ the o/p must progressively decreases toward zero

Here it is given as.

$$V_{o2} = V_p e^{-t'/RC} \quad \text{where } t' = t - t_p$$

$$\therefore V_{o2} = V_p e^{-(t-t_p)/RC}.$$

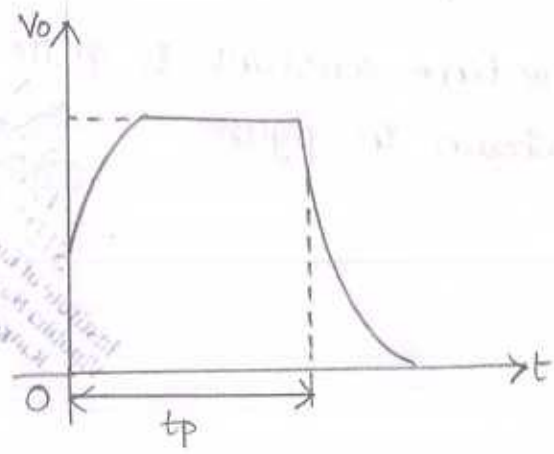
It is observed that there is marked distortion of the o/p voltage wave form. the o/p wave extends far beyond t_p, since some time must elapse before all the charge on the capacitor can leak away

In practise distortion of all the wave shape can be minimised by making the rise time t_r, small in comparsion with the pulse width t_p

The usual practice is to make the upper cut off frequency $f_2 = \frac{1}{t_p}$.

with $f_2 = 1/t_p$ we have $t_r = 0.35/f_2 = 0.35 t_p$

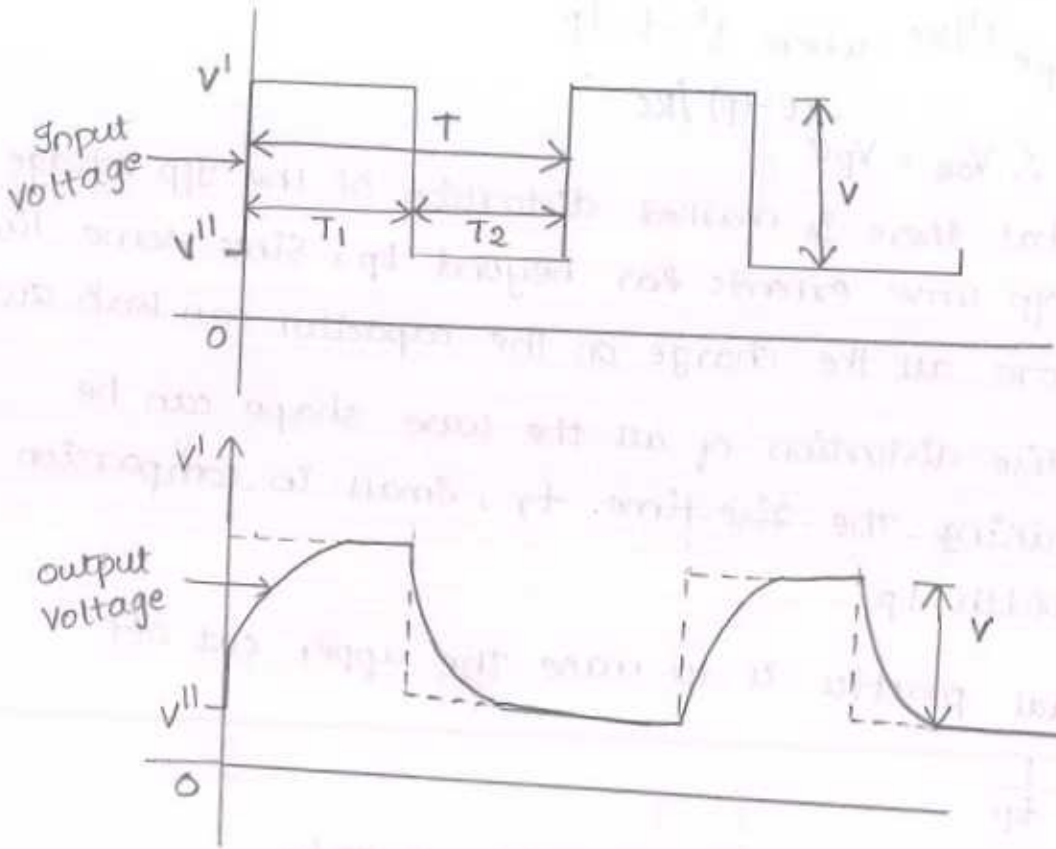
The o/p wave form is as shown in fig 2-34.



The deviation from the I/p wave form is quite small, and for all practical purpose it may be assumed that the pulse voltage retains its wave shape, provided the reciprocal of the pulse width is approximately equal to the upper 3-dB frequency.

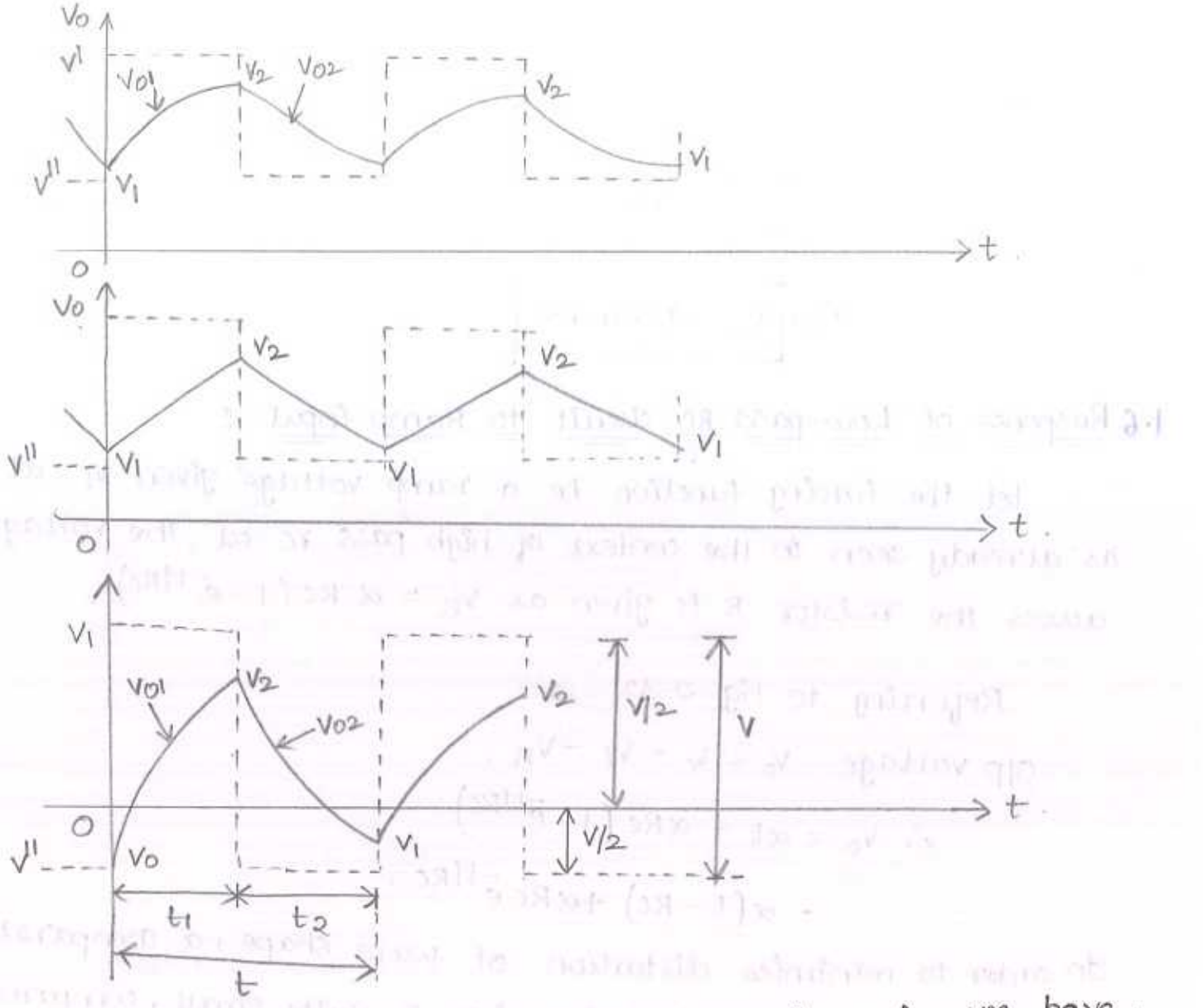
1.5 Response of low pass RC circuit to square wave input :

let the forcing function be a square-wave voltage shown in



If the rise time tr is quite small as compared to T, there is no marked distortion of wave form the out put wave form would be as shown in figure

If however, the time constant is quite large the o/p wave form would be shown in figure.



when the output voltage is exponentially increasing we, have, referring to fig.

$$V_{o1} = V' + (V_1 - V')\, e^{-t/RC}.$$

$$\left[\text{final value} + (\text{Initial value} - \text{final value})\, e^{-t/RC}\right]$$

when the o/p voltage is exponentially decreasing we have.

$$V_{o2} = V'' + (V_2 - V'')\, e^{-(t-T_1)/RC}$$

Also, it is seen that $V_{o1} = V_2$ at $t = T_1$ and V_{o2} at $t = T_2$. The time figure shows the wave form of the two o/p voltages whereby the time constant is very large compared to the periodic time. The exponential curves become practically linear.

If the i/p voltage is a symmetrical square wave.

we have $T_1 = T_2 = T/2$ and $V^1 = -V^{11} = V/2$

also $V_1 = -V_2$ It can be shown that

$$V_2 = \frac{V}{2}\left(\frac{e^{2x}-1}{e^{2x}+1}\right) \text{ where } x = \frac{T}{4RC}.$$

(or) $$\boxed{V_2 = \frac{V}{2}\tan hx}$$

1.6 Response of low-pass RC circuit to Ramp input :

Let the forcing function be a ramp voltage given $V_i = \alpha t$. as already seen in the context of high pass rc ckt, the voltage across the resistor R is given as $V_R = \alpha RC(1-e^{-t/RC})$.

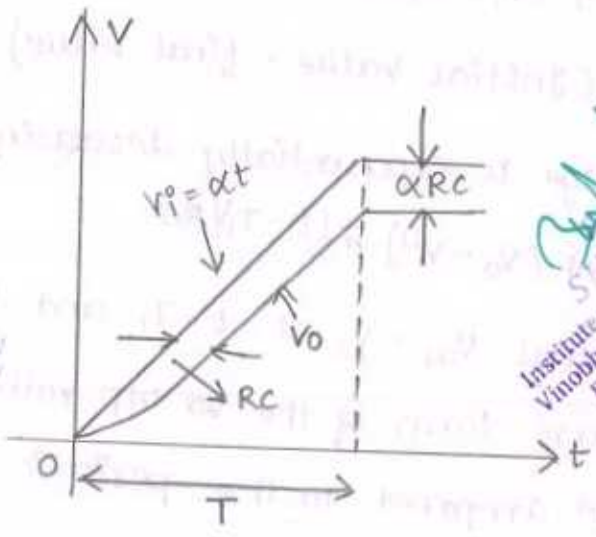
Referring to fig 2.32

o/p voltage $V_o = V_c = V_i - V_R$.

$$\therefore V_o = \alpha t - \alpha RC[1-e^{-t/RC}]$$

$$= \alpha(t-RC) + \alpha RC\, e^{-t/RC}.$$

In order to minimise distortion of wave shape, a comparatively small time constant is selected (Rc is quite small, compared to the total ramp time T) The o/p wave form is as shown in fig



It is seen that the wave form of the voltage is more (or) less preserved (There is a small amount distortion near t=0 only. Also, the o/p follows the input (except near the origin) but is delayed by one time constant (RC) In other word there is a difference of one time constant blw I/p and O/p

1.6.1 Transmission error (e_t) :-

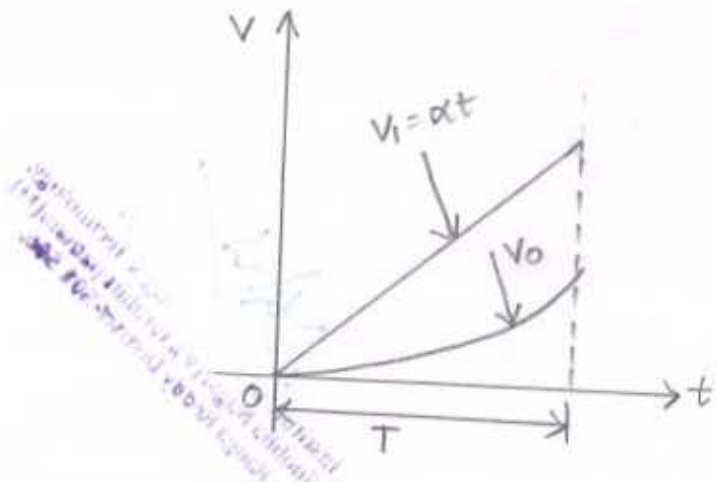
Referring in figure it is seen that there is a difference of one time constant RC blw the I/p and o/p. This difference usually expressed as a fraction of the I/p at the end of the ramp at $t = T$ (both in time units). It is termed as transmission error (e_t)

we have transmission error $e_t = \frac{RC}{t}$.

As already seen $f_2 = \frac{1}{2\pi RC}$ (or) $RC = \frac{1}{2\pi f_2}$

$$\boxed{e_t = \frac{1}{2\pi f_2 T}}$$

If the time constant is very large compared to T. there is very much distortion, and the o/p voltage curve is as shown in figure



As already obtained

$$V_0 = \alpha(t-RC) + \alpha RC\, e^{-t/RC}$$

If $RC \gg T$, it can be shown that

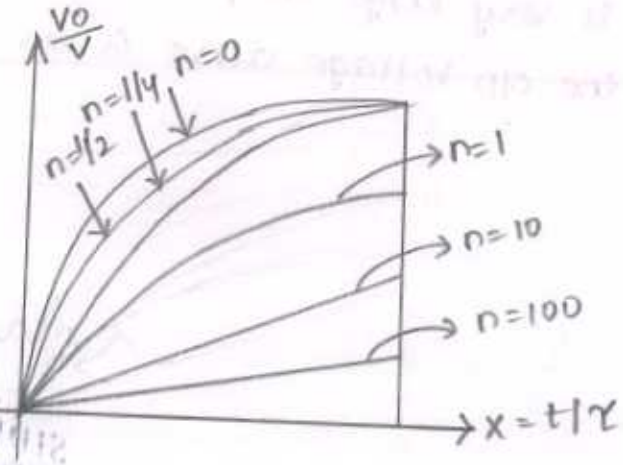
$$\boxed{V_0 = \frac{\alpha t^2}{2RC}}$$

The excitation is linear, but the response is quadratic, as is evident from the above expression. This circuit therefore acts as an integrator.

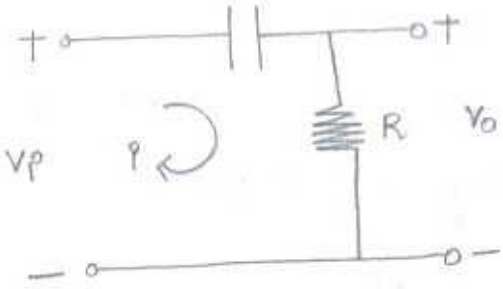
1.7 Response of Low-pass RC network to exponential input :-

If the forcing function is an exponential voltage of the form $V_f = V(1-e^{-t/RC})$ where V is the final (or) steady state value the o/p voltage is also an increasing exponential & its actual shape depends on the ratio $\frac{RC}{T} = n$ and the ratio $\frac{t}{T} = x$.

For different values of n, the output curves are as shown in figure.



1. High pass RC circuit :



let V_i = i/p signal.

V_o = o/p voltage.

The o/p is taken across the resistance R). Also let i denoted the circuit current.

If the i/p signal V_i is non-sinusoidal, it can be visualised as comprising of several sine wave of frequency which are multiples of the frequency of the signal, and there may be a d.c component also. Since the reactance of the capacitor decreases as the frequency increased $\left(X_C = \frac{1}{2\pi f C} \right)$.

Apply KVL to the circuit of fig, we have;

$V_C + V_R = V_i$ where V_c = voltage across the capacitor &
V_R = voltage across the resistance

But $V_C = \frac{1}{C}\int i\,dt$ and $V_R = V_o$ the o/p voltage.

$\therefore \frac{1}{C}\int i\,dt + V_o = V_i$

current $i = \frac{V_R}{R} = \frac{V_o}{R}$

$\therefore \frac{1}{C}\int \frac{V_o}{R}\,dt + V_o = V_i$.

differentiating wrt 't' the above eqn transforms into

$$\frac{1}{C}\left(\frac{V_o}{R}\right) + \frac{dV_o}{dt} = \frac{dV_i}{dt}$$

$$\left(\frac{1}{CR}\right) V_o + \frac{dV_o}{dt} = \frac{dV_i}{dt}$$

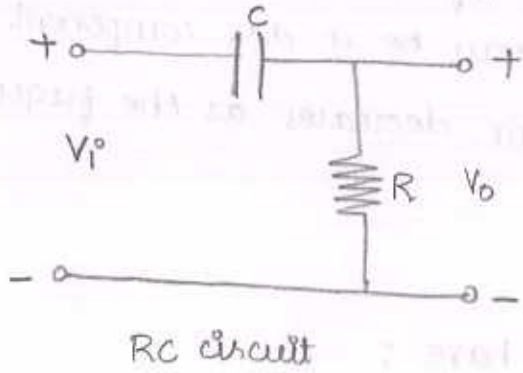
The total response of the ckt to the applied forcing function consists of transient response) and steady state response).

we have transient response $= \frac{dV_o}{dt}$ and

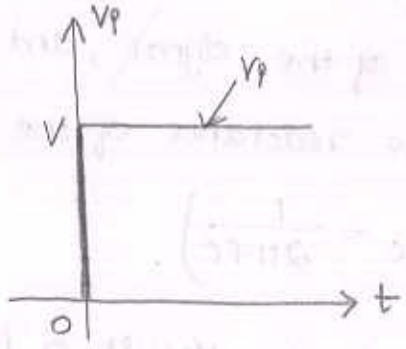
steady state response $= \left(\frac{1}{RC}\right) V_o$.

2.1 Response of high-pass RC circuit to step input :

Consider the RC circuit shown in figure. Let the forcing function be a step voltage V applied at $t = 0$.



RC circuit



step voltage input.

As already studied, the I/p and o/p of such a high pass RC circuit are related by the differential equation.

$$\left(\frac{1}{RC}\right) V_o + \frac{dV_o}{dt} = \frac{dV_i}{dt}$$

Since the input is a step voltage $V_i = V$ for $t > 0$.

$\therefore \frac{dV_i}{dt} = \frac{dV}{dt} = 0$ since V is of constant magnitude

$$\therefore \frac{dV_o}{dt} + \left(\frac{1}{RC}\right) V_o = 0.$$

The general solution to this equation is of the form.

V_0 = complementary function + particular function.

(i) The complementary function represents the transient response & is of the form $\left(Ke^{-t/RC}\right)$ where, as seen already $RC = \tau$ the time constant of the circuit.

(ii) The particular integral represents the steady state response. Since, under steady state conditions, the capacitor blocks the passage of dc, the o/p is zero. Hence the particular integral = 0.

$\therefore V_0 = Ke^{-t/RC}$ where K is a constant by applying initial conditions

At $t(0+)$ we have

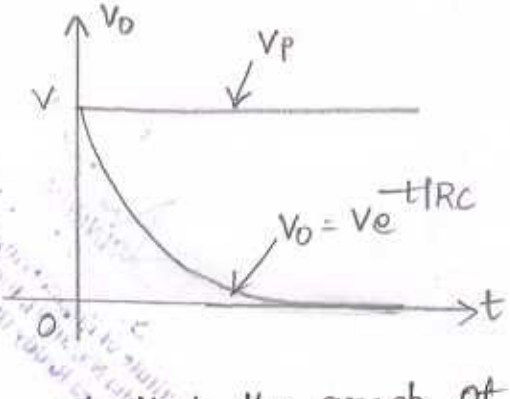
$V_0(0+) = Ke^0 = K$ putting $t = 0$.

But $V_0(0+) = V$ $\therefore K = V$.

Hence we get

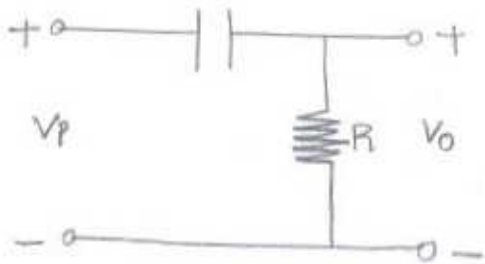
$$\boxed{V_0 = Ve^{-t/RC}}$$

The response characteristics

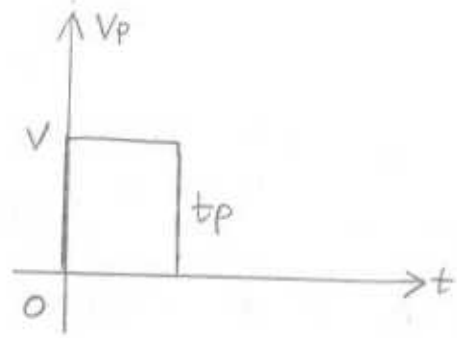


It is observed that the graph of V_0 't' is an exponentially decreasing curve. The voltage V_0 because practically zero after 5 time-constants.

2.2 Response of high pass RC circuit to pulse input :



RC circuit



pulse input wave form

let the input voltage be a pulse applied at $t = 0$.

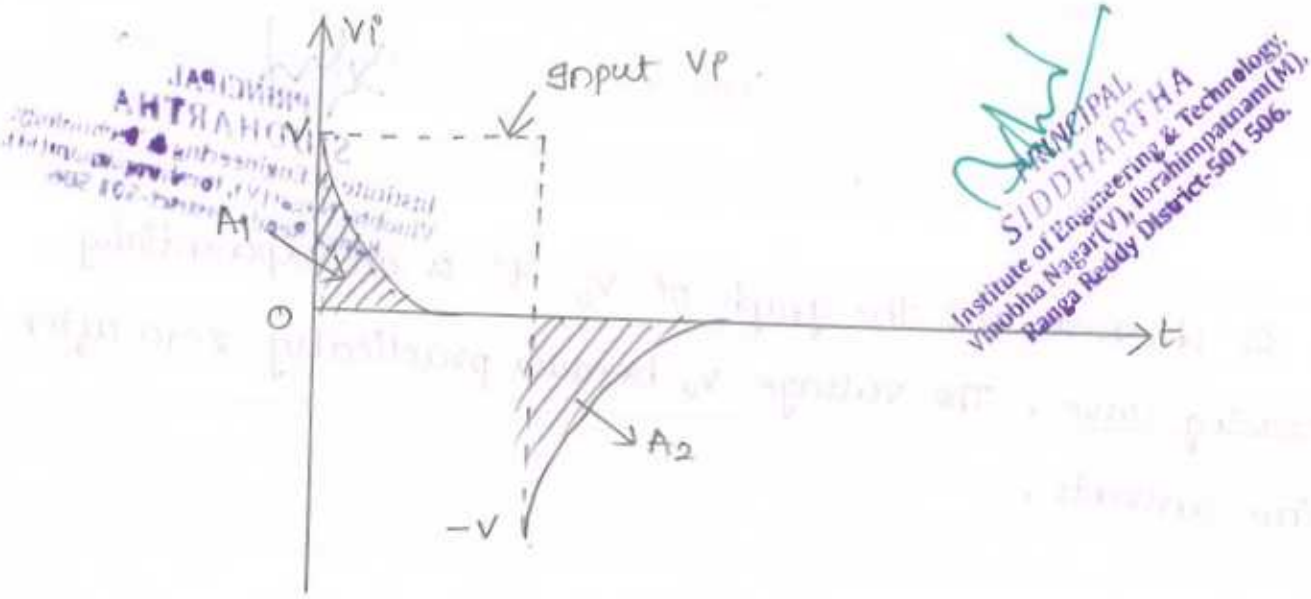
i) let the time constant are far less than the pulse width

ie, $RC << tp$ (or) $RC/tp << T$.

It is evident that the response of the ckt is the same as for a step input in the interve $0, t < tp$

~~It is evident that the~~

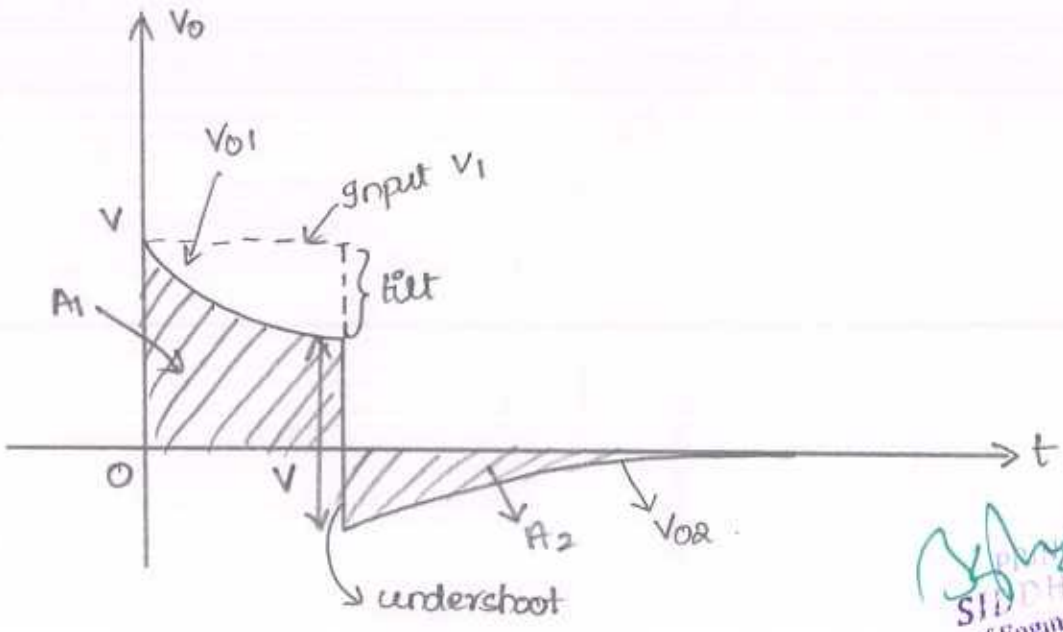
Hence the o/p must decay exponentially towards zero. since $RC << tp$ the transient state is quite small, Also at $t = tp$. the i/p voltage changes abruptly to zero. Thus V_o becomes $-V$ at $t = tp$ and exponentially.



The +ve area A_1 and the -ve area A_2 are always equal, This is due to the fact that under steady state conditions, the capacitor blocks dc & totally segregates the output & the I/P with the result that the average is zero.

In order to minimize ~~direction~~ distortion, it is abundantly clear that the time-constant of the ckt must be very large as compared to the pulse width.

Thus pulse can be converted into spikes by making the time constants quite small, and this process is termed as peaking

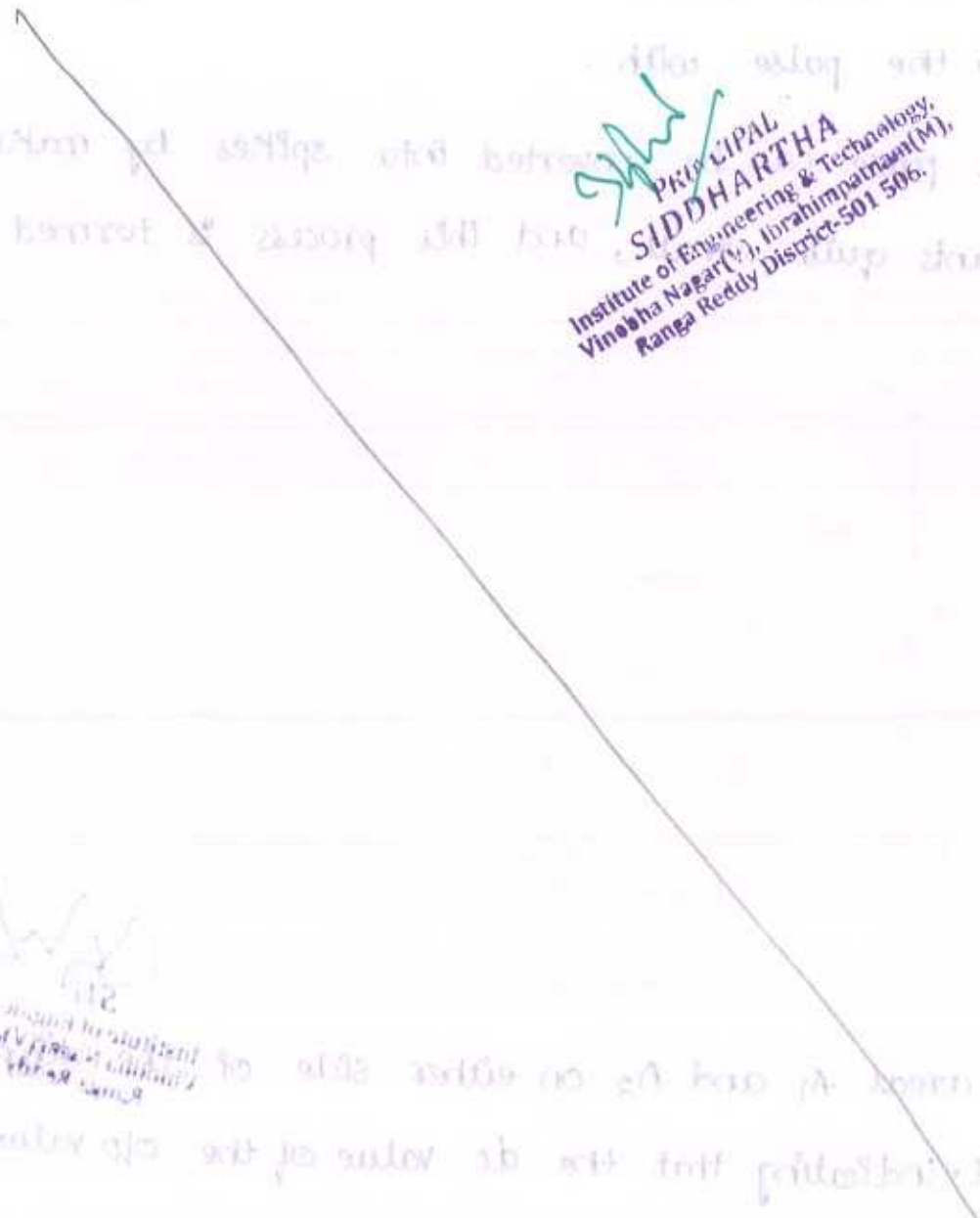


The two areas A_1 and A_2 on either side of the time axis are Equal. indicating that the dc value of the o/p value is zero.

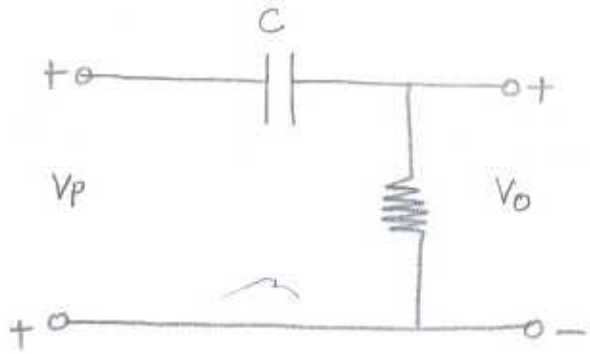
It may be noted that at the end of the pulse that at $t = t_p$. the I/P voltage V_i shows drops from V to zero.

abruptly, and the o|p voltage V_o also drops by the same amount V. and hence becomes negative.

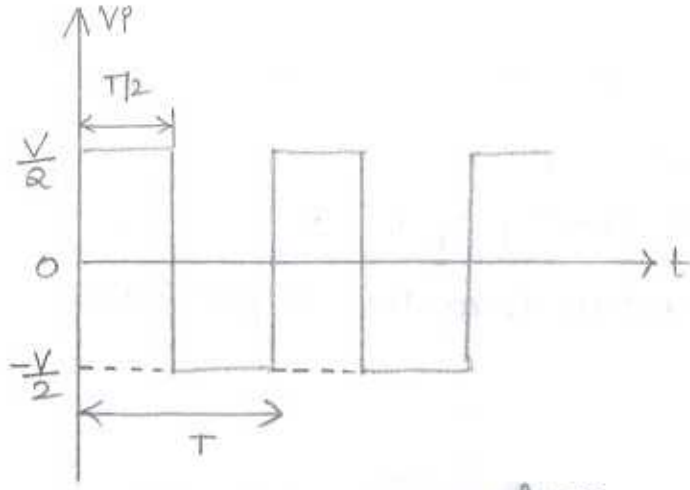
Thereafter it decays exponentially towards zero at such at rate that the area below the time axis is made equal to the area above the axis.



2.3 Response of high pass RC circuit to Symmetrical Square wave Input :-



HP RC circuit



I/p voltage wave form

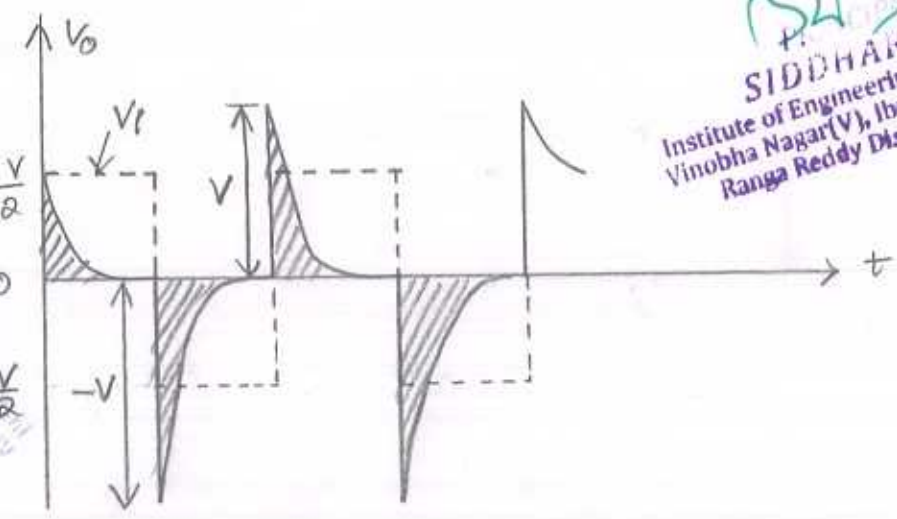
Let the forcing function be a symmetrical square value wave voltage of peak-to-peak amplitude V and period 'T'

Case (i) :- Let $RC << T$ ie, $\tau/T << 1$

At $t = T/2$ the input voltage drops from $+\frac{V}{2}$ to $-\frac{V}{2}$ abruptly, Hence the o/p voltage must also drops by the same amount ie V

$V_0 = -V$ at $t = T/2$ the voltage -V rapidly & exponentially towards Zero

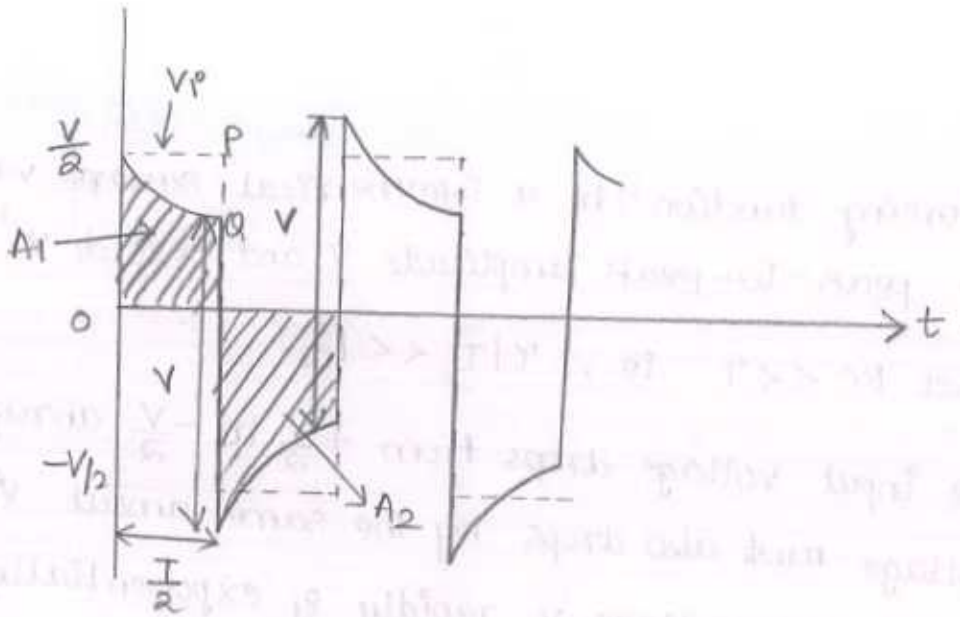
the i/p voltage rises abruptly to $+\frac{V}{2}$ from $-\frac{V}{2}$. Here the output voltage also rises instantaneously from 0 to +V and there after it begins to decay exponentially towards zero.



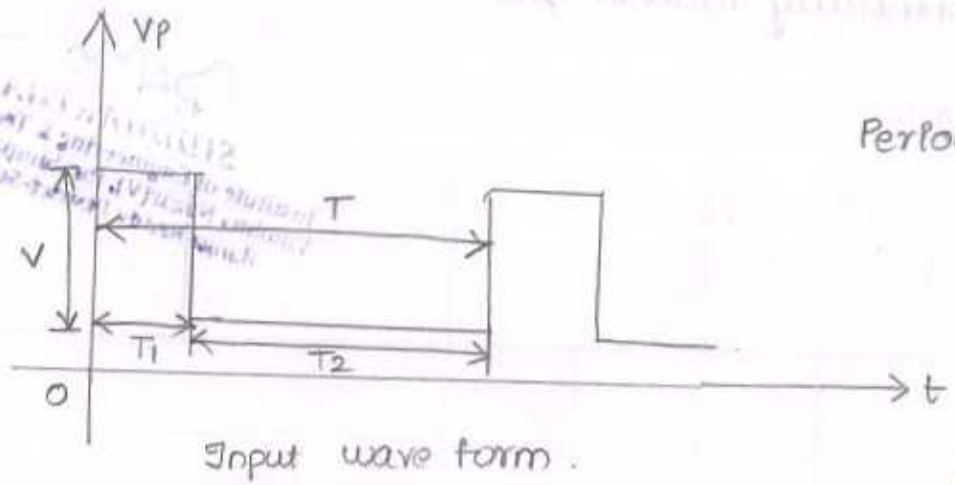
Case (ii)

Let $RC >> T$ ie $\tau/T >> 1$

If the time-constant is quite large, the exponential decay of the output voltage is slower as seen already. This results in a tilt at the top of the i/p wave & an undershoot at the bottom, as is obvious from the output wave.

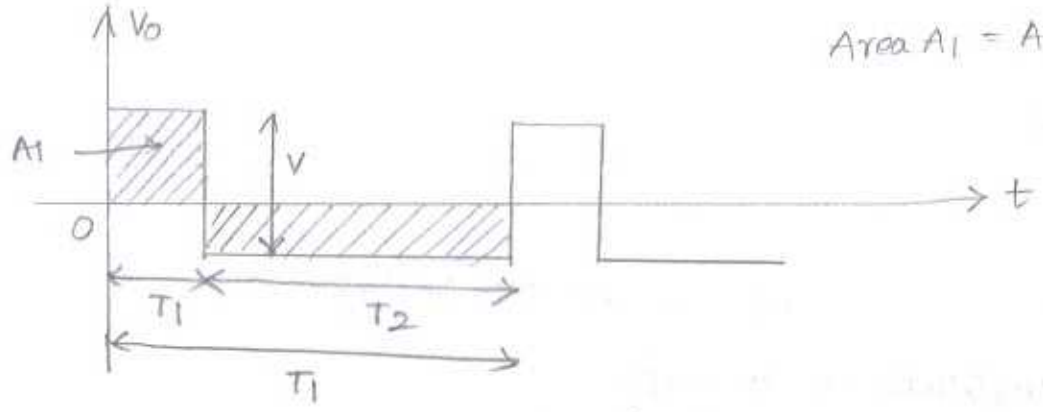


Areas A_1 and A_2 are equal, PQ = tilt at the top of the wave. If the i/p voltage is not symmetrical, and it the form shown in fig and the circuit has a very large time-constants. The response curve would be of the form in figure.



Input wave form.

Period $T = T_1 + T_2$



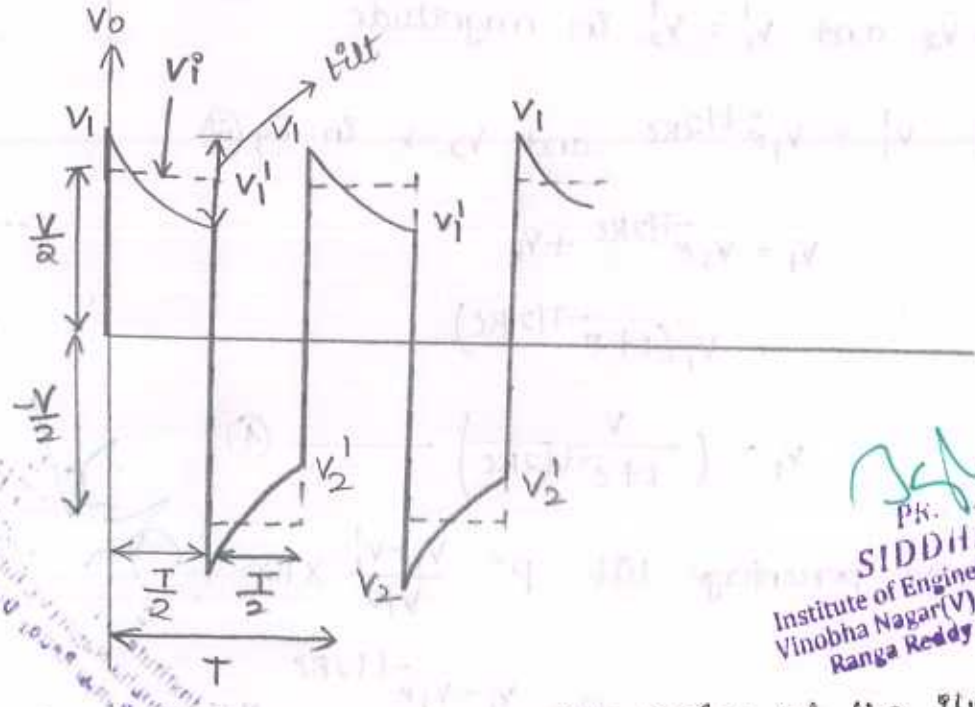
output wave form

There is no appreciable change in the wave form as such, but since the dc component of the o/p voltage is zero, the wave lies on b.s of the time axis, making the +ve and -ve areas equal.

3.1 Expression for percentage tilt :-

Consider the steady state response of a high pass RC circuit to a symmetrical square wave input. As

Assuming $RC >> T$, the output wave is as shown.



Thus it is seen that during a +ve swing of the i/p voltage its amplitude remains constant at V/2. since the decrease of the o/p is exponential & is quite slow ($RC >> T$) the amplitude drops from

from V_1 to V_1'

percentage tilt $P = \frac{V_1 - V_1'}{(V/2)} \times 100$.

It is the o/p amplitude decay expressed as a percentage of the i/p amplitude

Consider a +ve swing of the i/p voltage wave

we have amplitude of $V_i = V/2$

at $t = 0$, $V_0 = V_1$

The o/p decays according to exponential law

$\therefore$ for $t > 0$ $V_0 = V_1 e^{-t/RC}$ —— ①

At the end of the +ve swing

i.e, at $= T/2$, $V_0 = V_1'$

$\therefore V_1' = V_1 e^{-t/2RC}$, putting $t = T/2$ in Eq ① —— ②

we have $V = V_1' + V_2$ in magnitude —— ③

Also $V_1 = V_2$ and $V_1' = V_2'$ in magnitude

putting $V_1' = V_1 e^{-t/2RC}$ and $V_2 = V$ in Eq ③.

$$V_1 = V_1 e^{-T/2RC} + V_1$$

$$= V_1 (1 + e^{-T/2RC})$$

$$V_1 = \left(\frac{V}{1 + e^{-t/2RC}} \right) \text{ —— ④}$$

we have percentage tilt $P = \frac{V_1 - V_1'}{V/2} \times 100$

$$P = \frac{V_1 - V_1 e^{-t/2RC}}{V/2} \times 100$$

$$= \frac{2V_1 (1 - e^{-T/2RC})}{V} \times 100$$

putting $V_1 = \frac{V}{1+e^{-T/2RC}}$ from Eq ④ in above expression

we get $p = \frac{2V(1-e^{-T/2RC})}{(1+e^{-T/2RC}} \times 100$.

$= \frac{2(1-e^{-T/2RC})}{1+e^{-T/2RC}} \times 100$.

Hence the most general form of the expression for tilt is

$$\% \text{ tilt } P = \frac{1-e^{-T/2RC}}{1+e^{-T/2RC}} \times 200$$

If $RC >> T$, $\frac{RC}{T} >> 1$ (or) $\frac{T}{RC} << 1$

also $\frac{T}{2RC} << 1$

$\therefore e^{-T/2RC} \cong 1 - \frac{T}{2RC}$ Since $e^x \cong 1-x$ for $x << 1$

putting $e^{-T/2RC} = 1 - \frac{T}{2RC}$ in the above expression for P

we get $\%$ tilt $P = \frac{1-(1-T/2RC)}{1+(1+T/2RC)} \times 200$

(or) $p = \frac{T/2RC}{2+T/2RC} \times 200$.

$= \frac{T/2RC}{2} \times 200$.

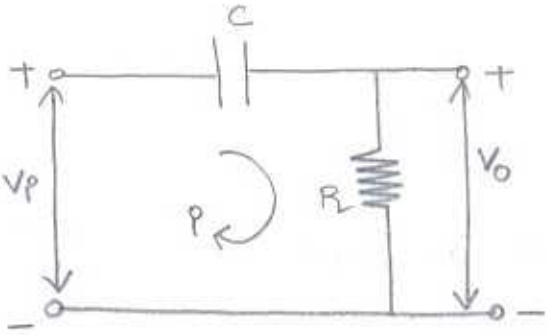
Since $\frac{T}{2RC} << 1$ and hence can be ignored .

$= \frac{T}{2RC} \times 100$

$$\boxed{\% \text{ tilt} = \frac{T}{2RC} \times 100\%}$$

2.3.2 Relationship between f_1 and γ :

consider the RC circuit



Let V_i be the input voltage and V_o the output voltage.

the ratio $\left(\frac{V_o}{V_i}\right)$ is termed as voltage gain it is denoted by A.

$\therefore$ we have $A = \left|\frac{V_o}{V_i}\right|$

If the i/p voltage V_i is sinusoidal, the o/p voltage is V_o is also sinusoidal and there will be no distortion of wave form. As the frequncy increases. The capacitance ive reactance of C $[X_C = 1/2\pi fC]$

Hence the total circuit impedance reduces & current increases.

we have current $I = \frac{V_i}{Z_{total}}$ where

$$Z_{total} = R - jX_C$$

$$= R - j\left(\frac{1}{2\pi fC}\right)$$

Output voltage $V_o = IR$

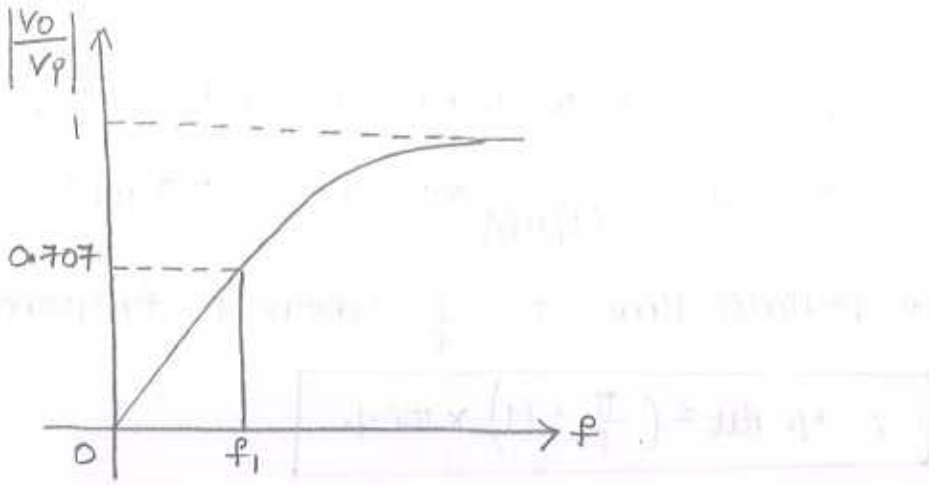
$$= \frac{V_i R}{Z_{total}}$$

$$\frac{V_o}{V_i} = \frac{R}{Z_{total}} = \frac{R}{R - j\left(\frac{1}{2\pi fC}\right)}$$

$$\frac{V_o}{V_i} = \frac{1}{1 - j\left(\frac{1}{2\pi fRC}\right)}$$

Magnitude of $\frac{V_o}{V_i} = \left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{1+\left(\frac{1}{2\pi fRC}\right)^2}}$

The graph voltage gain $\left|\frac{V_o}{V_i}\right|$ plotted against frequency 'f' is as shown



At $f = f_1$ the voltage gain is $\frac{1}{\sqrt{2}}$ (or) 0.707 of the maximum value.

f_1 is the lower cut-off frequency.

putting $f = f_1$ and $\left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{2}}$ and the expression we get

$$\frac{1}{\sqrt{2}} = \frac{1}{\sqrt{1+\left(\frac{1}{2\pi f_1 RC}\right)^2}}$$

$$\sqrt{2} = \sqrt{1+\left(\frac{1}{2\pi f_1 RC}\right)^2}$$

$$(\sqrt{2})^2 - 1 = \left(\frac{1}{2\pi f_1 RC}\right)^2$$

$$1 = \frac{1}{2\pi f_1 RC}$$ taking square roots.

$$\therefore f_1 = \frac{1}{2\pi RC} \quad (\text{or}) \quad f_1 = \frac{1}{2\pi\tau} \qquad \therefore RC = \tau$$

This is the relationship obtaining between the lower cut off frequency f_1 and time constant τ.

2.3.4 Relationship between f_1 and percentage tilt :

we have % tilt $= \frac{T}{2RC} \times 100$.

also $f_1 = \frac{1}{2\pi RC}$ from which $2RC = \frac{1}{\pi f_1}$

Sub this values in the expression for tilt, we get

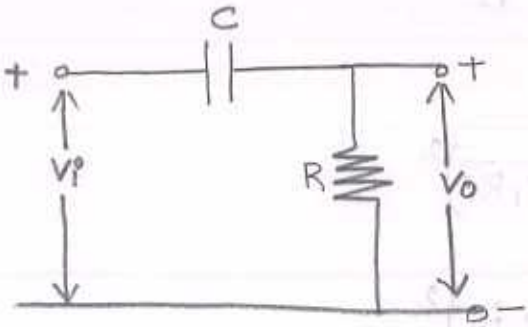
$$\% \text{ tilt} = \frac{T}{(1/\pi f_1)} \times 100\% = (\pi T f_1) \times 100\%$$

But the periodic time $T = \frac{1}{f}$ where f = frequency in Hz.

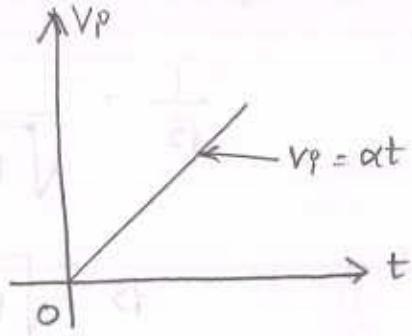
$$\therefore \% \text{ tilt} = \left(\frac{\pi}{f} \cdot f_1\right) \times 100\%$$

2.4 Response of high pass RC circuit to ramp input :

consider the RC circuit of fig excited by a ramp ~~signal~~ voltage. Let the input voltage $V_i = \alpha t$.



RC circuit



Input ramp voltage wave form

we studied that for the circuit under consideration

$$\left(\frac{1}{RC}\right) V_o + \frac{dV_o}{dt} = \frac{dV_i}{dt}$$

putting $V_i = \alpha t$, we get

$$\left(\frac{1}{RC}\right) V_o + \frac{dV_o}{dt} = \frac{d}{dt}(\alpha t) = \alpha$$

The sol^n to the diff eqn is of the form

V_o = complimentary fun + particular integral

(i) The particular integral representation the forced (or) steady state response is constant, and as such, its derivation is zero. Hence putting V_0 = particular integral, we get.

$$\left(\frac{1}{RC}\right) \text{particular integral} + 0 = \alpha .$$

$$\text{particular integral} = \alpha RC .$$

(ii) complementary function $= Ke^{-t/RC}$ where K is constants whose value can be computed by applying initial condition.

we have at $t = (0+)$ $V_0 = V$ $[V_0(0+) = V_0(0-) = 0]$.

$$\therefore 0 = Ke^{-t/RC} + \alpha RC .$$

$$= Ke^{0} + \alpha RC \quad \text{putting } t = 0 .$$

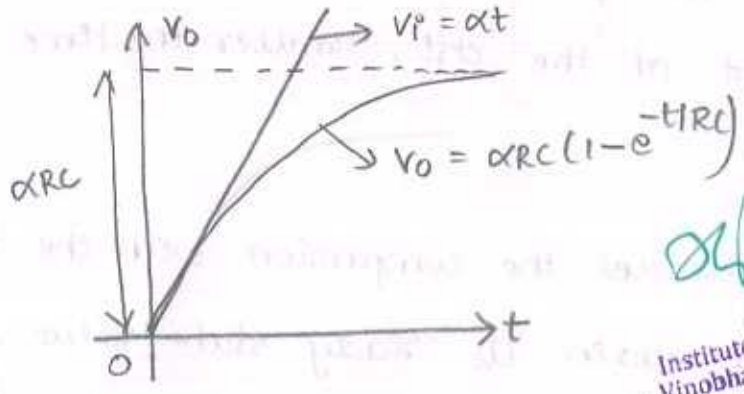
$$= K + \alpha RC .$$

$$(\text{or}) \quad = K - \alpha RC .$$

$\therefore$ The complete solution is $V_0 = -\alpha RCe^{-t/RC} + \alpha RC$

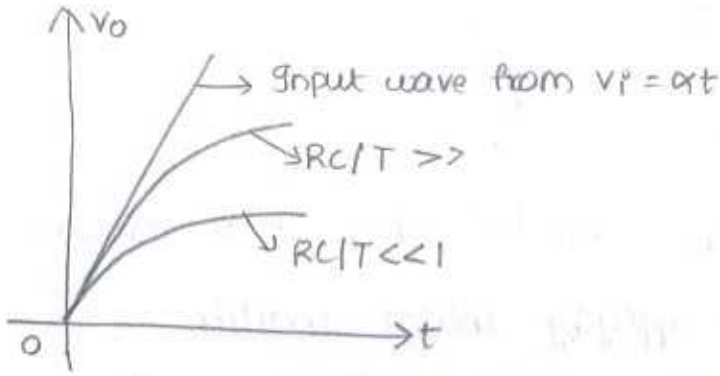
$$(\text{or}) \boxed{V_0 = \alpha RC(1 - e^{-t/RC})}$$

the response characteristics is as shown Fig.



From the expression for V_0 it is evident that for ramp I/P, the o/p curve is an increasing exponential.

If $RC/T >> 1$ the deviation of the o/p from linearity is quite small. But if $RC/T << T$ there is a marked deviation, as is obvious from the curve of fig.



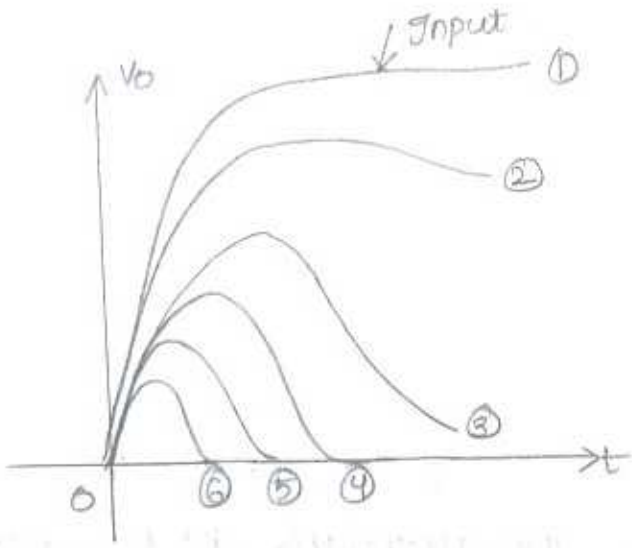
2.5 Response of high pass RC circuit to exponential input :-

It was seen earlier that for non-sinosoidal input voltage like step, ramp, square wave, pulse etc., the output voltage is exponential in nature. In particular, for a ramp input, the o/p voltage is exponentially rising and its wave form practically coincides with the i/p wave form near $t = 0$.

If the forcing function also an exponentially rising voltage, it is obvious that the o/p and i/p wave form are coincident at and near $t = 0$. The peak value of the o/p is decided by the and the time constant of the ckt. Smaller the time constant smaller the o/p peaks.

As T increases the comparsion with the time req for the i/p voltage to attain its ready state value, the o/p peaks also increases, as shown in fig. However the o/p voltage decays exponentially to zero.

→



1. I/p curve 1 is i/p curve 2 to 6 are o/p curves

3. Attenuators :

consider the simple resistive ckt shown in the figure.

V_i = I/p voltage and.

V_o = o/p voltage.

If 'i' is the ckt current, we have $i = \frac{V_i}{R_1+R_2}$

output voltage $V_o = iR_2 = \left(\frac{V_i}{R_1+R_2}\right) R_2$

$$V_o = \left(\frac{R_2}{R_1+R_2}\right) V_i .$$

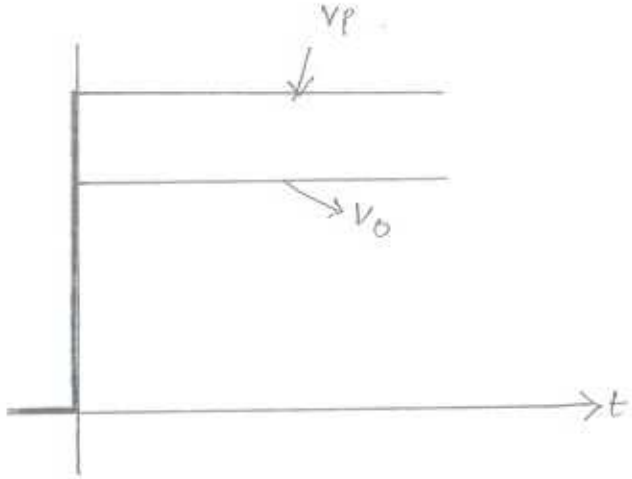
$a V_i$ & putting $\frac{R_2}{R_1+R_2} = a$.

Hence, the o/p is 'a' times the input.

The I/p signal gets multiplied by the ratio

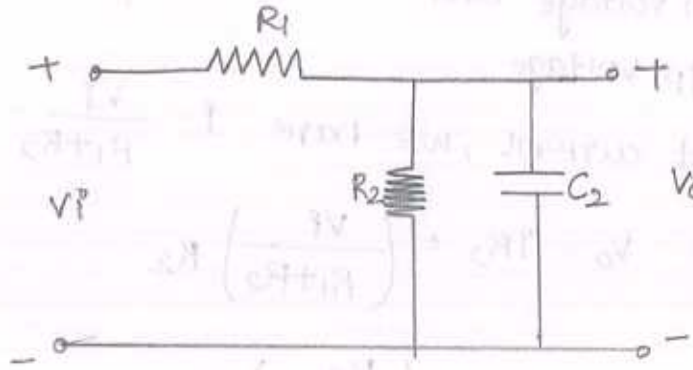
$$a = \frac{R_2}{R_1+R_2} .$$

The I/p and o/p wave forms are shown in fig. 2.1 (a) & (b) the input signal to be a step voltage.



In the above discussion, the attenuator ckt is considered to be a purely resistive ckt.

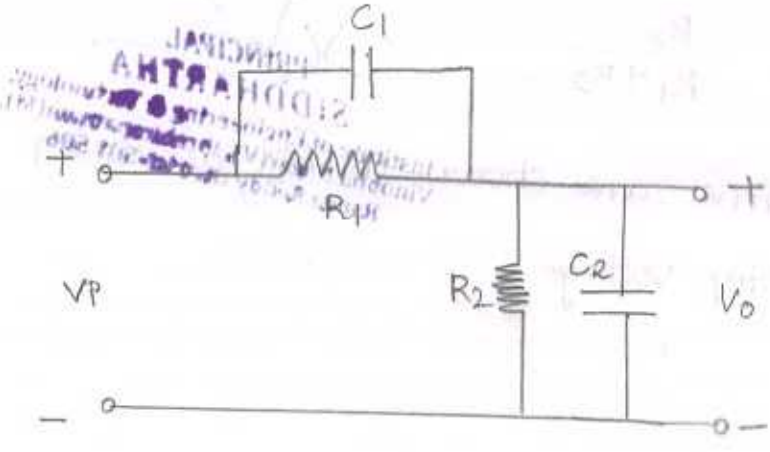
The attenuator ckt gets modified accordingly as in fig.



Thus in practice in a compensated attenuator a capacitor C_1 is put across, the resistor R_1 and its value is such that

$$R_1C_1 = R_2C_2$$

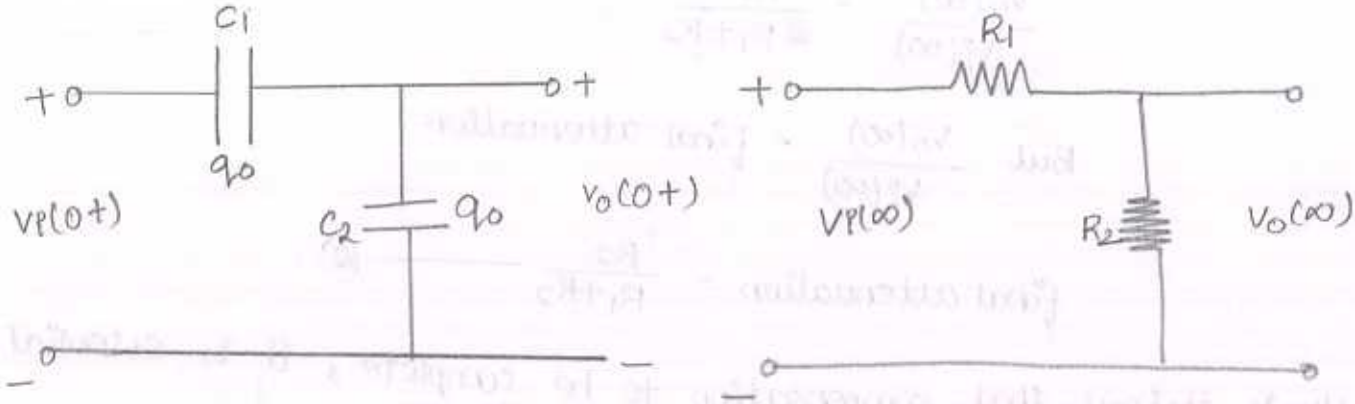
consider the compensated attenuator shown in fig.



It is shown that the undesirable effect of the distributed capacitance C_2 can be neutralised, and distortion of signal wave form prevented if $R_1C_1 = R_2C_2$.

Proof :-

(1) At $t = (0+)$ Immediately after the i/p signal is applied, the capacitance acts as short ckts and hence the resistance go out of ckt. The ckt modifies as shown in fig.



The capacitor get charged. Let q_0 denoted the charge on each capacitor at $t = t(0+)$

$$\therefore q_0 = C_2 V_o(0+) \quad (\text{or}) \quad V_o(0+) = \frac{q_0}{C_2}.$$

$$\text{also,} \quad V_i(0+) = \frac{q_0}{C_1} + \frac{q_0}{C_2} = q_0\left[\frac{1}{C_1} + \frac{1}{C_2}\right]$$

$$V_i(0+) = q\left[\frac{C_1 + C_2}{C_1 C_2}\right]$$

$$\text{Initial condition} = \frac{V_o(0+)}{V_i(0+)}$$

$$= \frac{q_0/C_2}{q_0\left[\frac{C_1+C_2}{C_1C_2}\right]}$$

$$= \frac{C_1}{C_1+C_2} \quad \text{——— (1)}.$$

(ii) $t = \infty$:-

at $t = \infty$, steady state has been reached. The capacitors acts as open-ckt & the ckt modifies as shown.

we have O/P $V_0(\infty) = iR_2$

$$\text{current } i = \frac{V_i(\infty)}{R_1+R_2}$$

$$\therefore V_0(\infty) = \left(\frac{V_i(\infty)}{R_1+R_2}\right) R_2$$

$$\frac{V_0(\infty)}{V_i(\infty)} = \frac{R_2}{R_1+R_2}$$

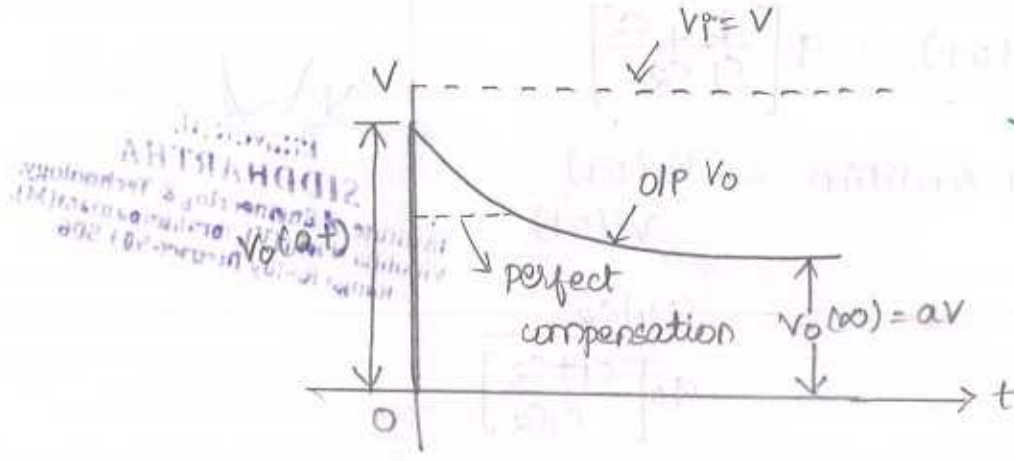
But $\frac{V_0(\infty)}{V_i(\infty)}$ = final attenuation.

$$\text{final attenuation} = \frac{R_2}{R_1+R_2} \quad \text{——— (2)}.$$

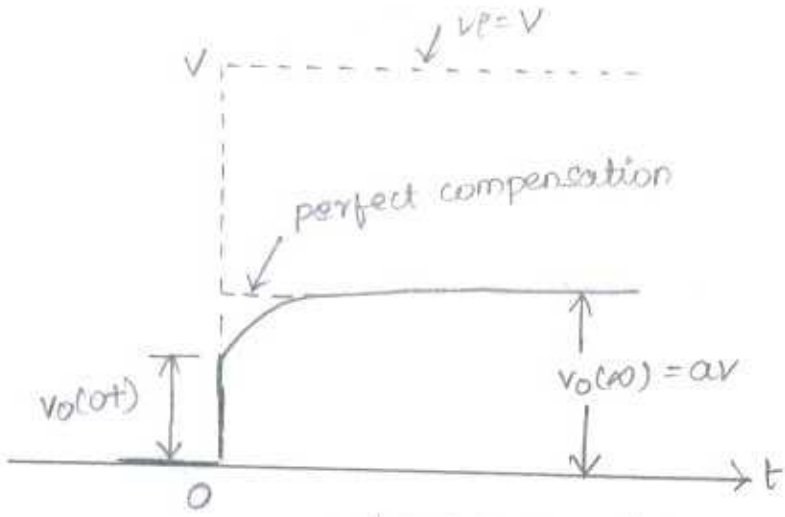
It is obvious that compensation to be complete, it is essential that initial attenuation = final ∞ attenuation.

$$\therefore \frac{C_1}{C_1+C_2} = \frac{R_2}{R_1+R_2} \quad \text{from (1) and (2)}.$$

simplifing we get $\boxed{C_1R_1 = C_2R_2}$



a) over compensation.



under compensation

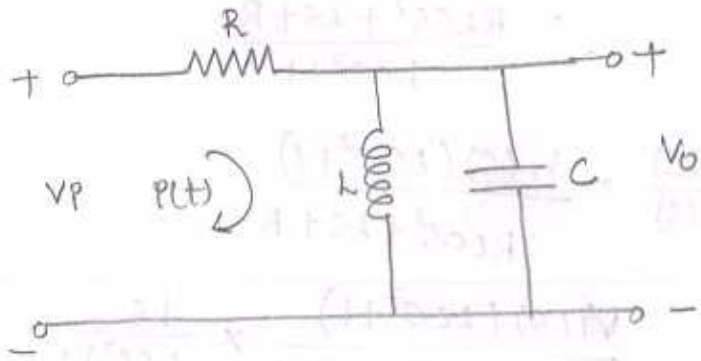
The condition $C_1R_1 = C_2R_2$ enables us to visuatise the practial attenuator ckt.

4. RL circuit :-

The time constant of such circuit is given as $\tau = RC$ if the resistance 'R' is replaced by an inductance L, and the capacitance C is replaced by a resistance R' such that time constant $\left[\frac{L}{R'}\right]$ of the new RL ckt is the same as that of the previously consided RC ckt $\left(\frac{L}{R'} = \tau = RC\right)$ then all the result obtained in relation to the RC ckt also hold good for the RL ckt.

5.0 RLC circuit :-

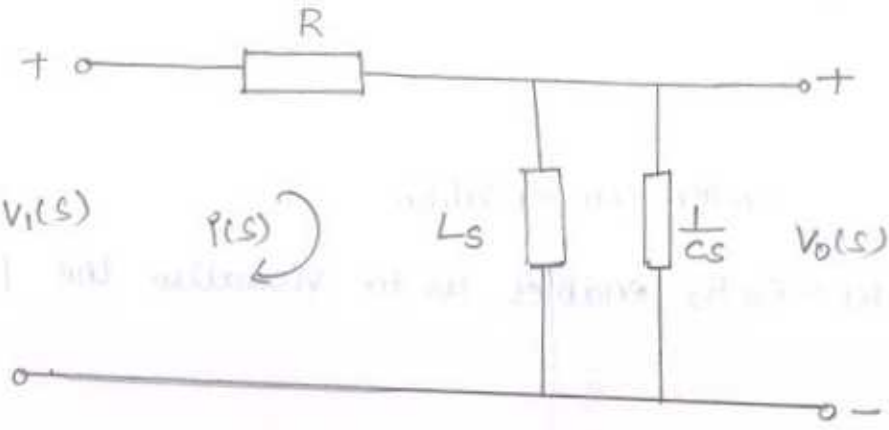
consider the RLC ckt.



let a signal V_i be applied to the RLC parallel ckt through the resistor R.

let V_o denoted the output

let i(t) denote the current with results.



Impedance transform of ;

R is R,

L is sL and

C is 1/cs.

Ls and 1/cs impedances are parallel.

their equivalent impedance $Z_{LC}(s) = \frac{(Ls)(1/Cs)}{Ls + 1/Cs}$.

$= \frac{Ls}{s^2LC+1}$ on simplification

total circuit impedance $Z(s) = R + \frac{Ls}{s^2LC+1}$

$= \frac{RLCs^2 + Ls + R}{LCs^2+1}$

$\therefore$ current $I(s) = \frac{V_i(s)}{Z(s)} = \frac{V_i(s)(LCs^2+1)}{RLCs^2+Ls+R}$.

output $V_o(s) = I(s) \cdot Z_{LC}(s) = \frac{V_i(s)(LCs^2+1)}{(RLCs^2+Ls+R)} \times \frac{Ls}{LCs^2+1}$

=

$$\frac{V_o(s)}{V_i(s)} = \frac{Ls}{RLCs^2+Ls+R}$$

$RLCs^2+Ls+R=0$ is the characteristics Equation.

The roots of this quaratic Eqn are:

$$s_1 = \frac{-L \pm \sqrt{L^2-4(RLC)R}}{2RLC} \text{ and}$$

$$s_2 = \frac{-L-\sqrt{L^2-4(RLC)R}}{2RLC}$$

$$s_1 = -\frac{1}{2RC} + \sqrt{\left(\frac{1}{2RC}\right)^2 - \frac{1}{LC}} \text{ and}$$

$$s_2 = -\frac{1}{2RC} - \sqrt{\left(\frac{1}{2RC}\right)^2 - \frac{1}{LC}} \text{ on simplification}$$

we have damping constants $K = \frac{1}{2R}\sqrt{\frac{L}{C}}$ and the natural frequency $f_0 = \frac{1}{2\pi\sqrt{LC}}$ & undamped period $T_0 = \frac{1}{f_0} = 2\pi\sqrt{LC}$

In terms of K and T_0 we get, on simplification.

$$s_1 = -\frac{2\pi K}{T_0} + j\frac{2\pi}{T_0}\sqrt{1-K^2} \text{ and}$$

$$s_2 = -\frac{2\pi K}{T_0} - j\frac{2\pi}{T_0}\sqrt{1-K^2}$$

Several cases arise, depending on the value of K.

1) If $K=0$, $s_1 = \pm j\frac{2\pi}{T_0}$ and $s_2 = -j\frac{2\pi}{T_0}$

Both roots s_1 and s_2 are imaginary and the response is an undamped sinusoid of time period T_0.

(ii) If $K=1$, $s_1 = s_2$ the two roots are Equal. This represents critical damping.

(iii) If $K>1$; the ckt becomes overdamping and there are no oscillations of the output.

(iv) If $K<1$; the output is a sinusoid whose amplitude whose amplitude progressively decays with time.

This represents underdamped response.

let Q = Q-factor of the parallel ckt comprising of R, L and C.

we have $Q = 2\pi f_0 RC = \frac{2\pi RC}{T_0}$ since $f_0 = \frac{1}{T_0}$.

$$= \frac{2\pi RC}{2\pi\sqrt{LC}} = \frac{RC}{\sqrt{LC}} = R\sqrt{\frac{C}{L}}.$$

but $\frac{1}{2R}\sqrt{\frac{L}{C}} = K$, from $R\sqrt{\frac{C}{R}} = \frac{1}{2K}$.

$$\boxed{\therefore Q = \frac{1}{2K}}$$

let the forcing function be a step voltage of magnitude V. let it be assumed that the ckt is relaxed at $t=0-$ ie, there is no initial inductor current (or) initial capacitor voltage.

$$\text{put } x = \frac{t}{T_0}.$$

It can be shown that;

(i) For critical damping if $K=1$,

$$\frac{V_0}{V} = 4\pi x e^{-2\pi x}$$

$$\frac{V_0}{V} = \frac{4Rt}{L} e^{-2Rt/L}$$

UNIT - II

Non-linear wave shaping:

2.1 Diode clippers:-

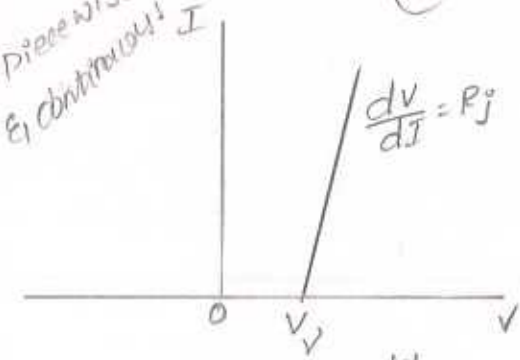
A diode volt-ampere characteristic may be approximated by a curve which is piecewise plinear & continuos. This idealised diode characteristic exibits a discontinuity in slope at the voltage. V_γ and this point of slope discontinuity is called breakpoint.

→ The break point occurs at $V_\gamma \approx 0.2$ V for Ge, & $V_\gamma \approx 0.6$V for Si.

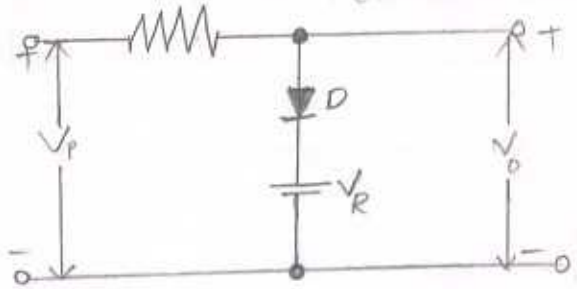
→ Using piecewise linear model of the diode we find clipping circuit

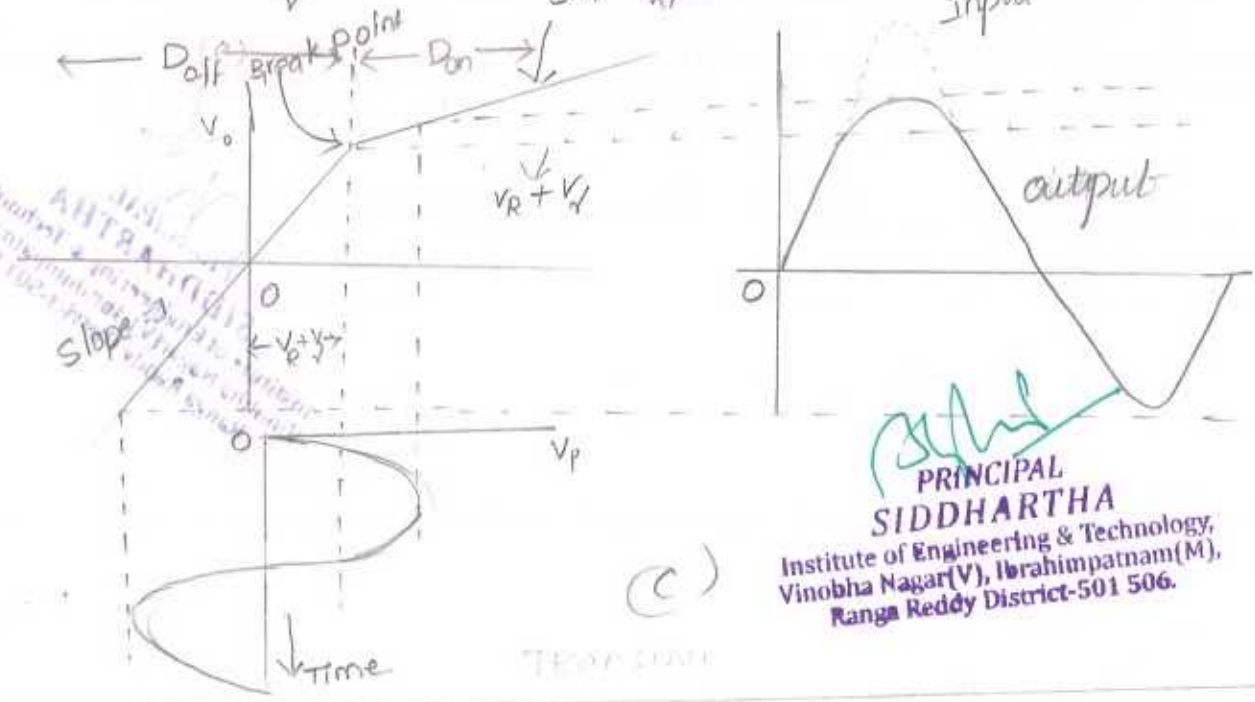
→ A break point occurs at the voltage $V_R + V_\gamma$.

(a)



(b) Transmission characteristic ckt





(c)

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Vinobha Nagar(V), Ibrahimpatnam(M),
Ranga Reddy District-501 506.

this above dig $V_0(t)$ is a Output voltage & $V_i(t)$ is input voltage

The break point $V_0(t) < V_R + V_\gamma$ - the diode is reverse biased (OFF)

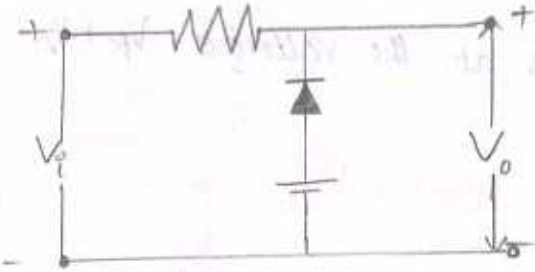
$$\Delta V_0(t) = \Delta(t) R_f / (R_f + R).$$

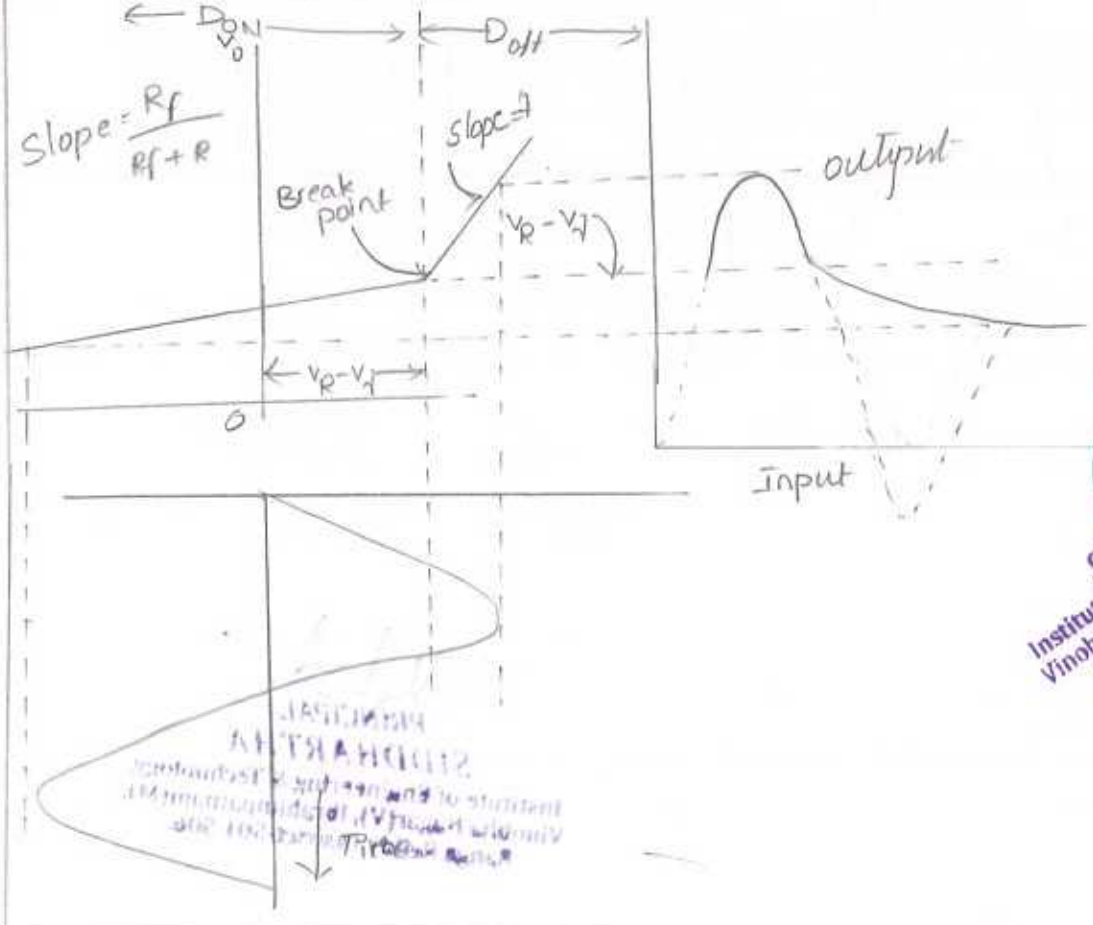
R_f is the diode forward resistance.

The corresponding o/p exibits a suppression of the +ve peak of the signal.

If $R_f << R$, then this suppression will be very pronounced.

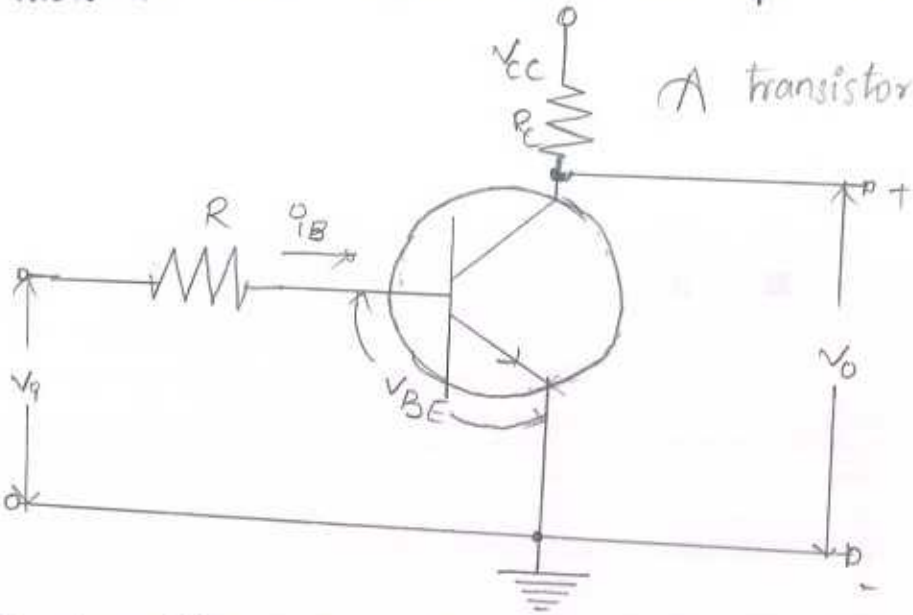
The o/p will appear as though the +ve peak had been clipped off or sliced off. it turns out that $V_R >> V_\gamma$ in this case one may consider that V_R itself is the limiting reference voltage.





2.2 The transistor clipper:

The transistor has two pronounced nonlinearities which may be used for clipping purposes. One occurs as the transistor crosses from cut-off into the active region, and second occurs when the transistor crosses from the active region to saturation.



A transistor clipper

The transistor enters its active region, the input impedence is approximately the short circuit input resistance hie.

$$hie = r_{bb'} + r_{b'e} = r_{bb'} + \frac{hfe}{gm}$$

$r_{bb'}$ is base-spreading resistance,

hfe is short-circuit common-emmitter current gain,

gm is the transconductance

$$hie = r_{bb'} + (hfe+1)\left(\frac{\eta V_T}{|I_E|}\right)$$

for an n-p-n germanium transistor. The slope $dv_{BE}(t)/dt$ of the base waveform is related to the slope $dv_i(t)/dt$ of the input by.

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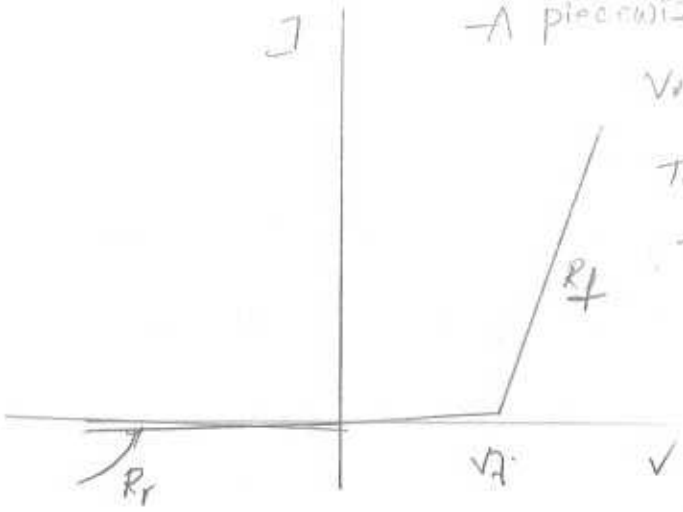


A piecewise linear & continuous approximation Volt ampere of semiconductor diode.

To the right of V_γ the forward resistance R_f is small, & left the reverse resistance R_r is large.

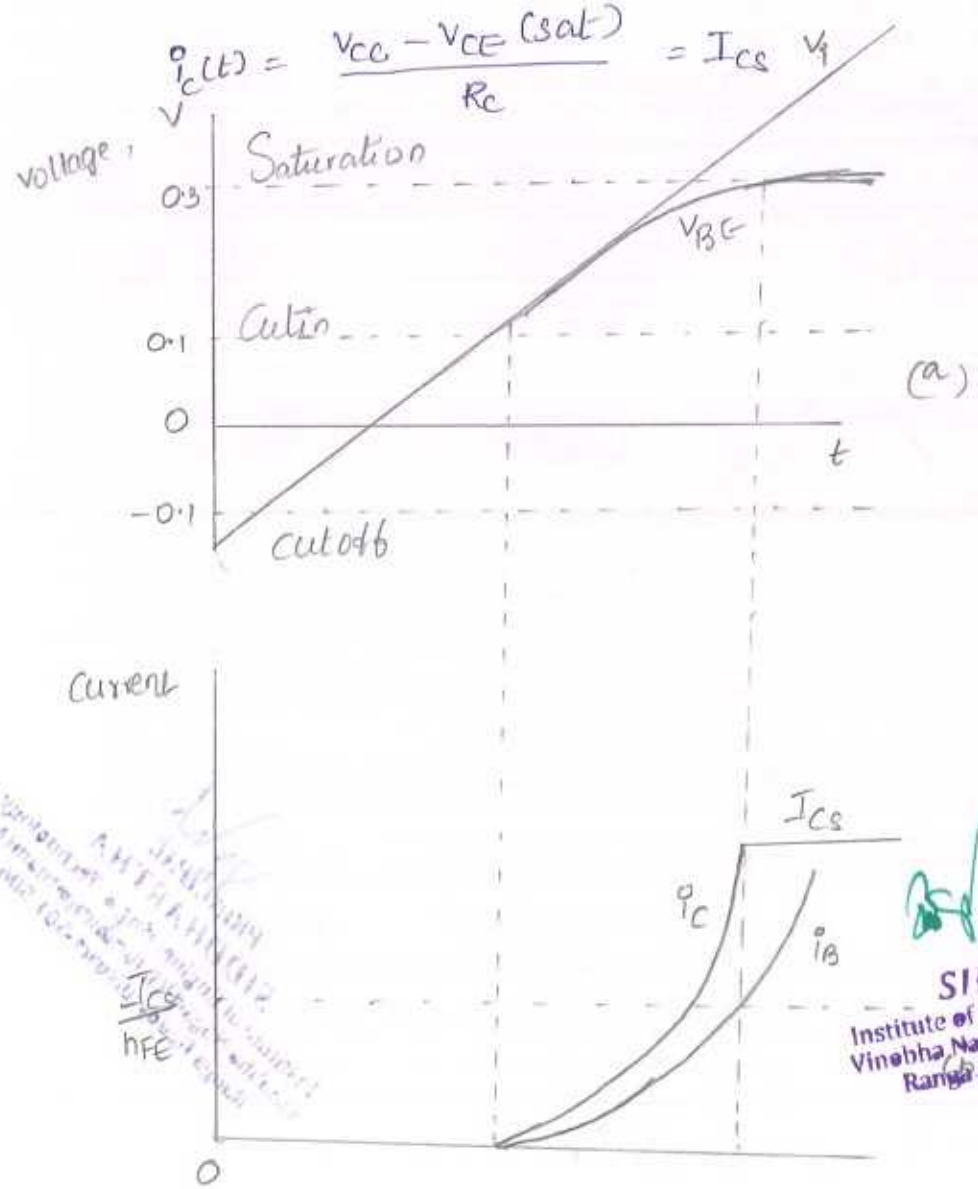
$$\frac{dv_{BE}(t)}{dt} = \frac{hie}{R+hie}\frac{dv_i(t)}{dt}$$

The input impedance hie decreases as the transistor goes further into the active region. Consequently the slope of $dv_{BE}(t)/dt$ decreases.

The slope of the base current $i_B(t)$ is given by.

$$\frac{di_B(t)}{dt} = \frac{1}{R+hie}\frac{dv_i(t)}{dt}$$

$$i_C(t) = \frac{V_{CC} - V_{CE}(sat)}{R_C} = I_{CS}$$

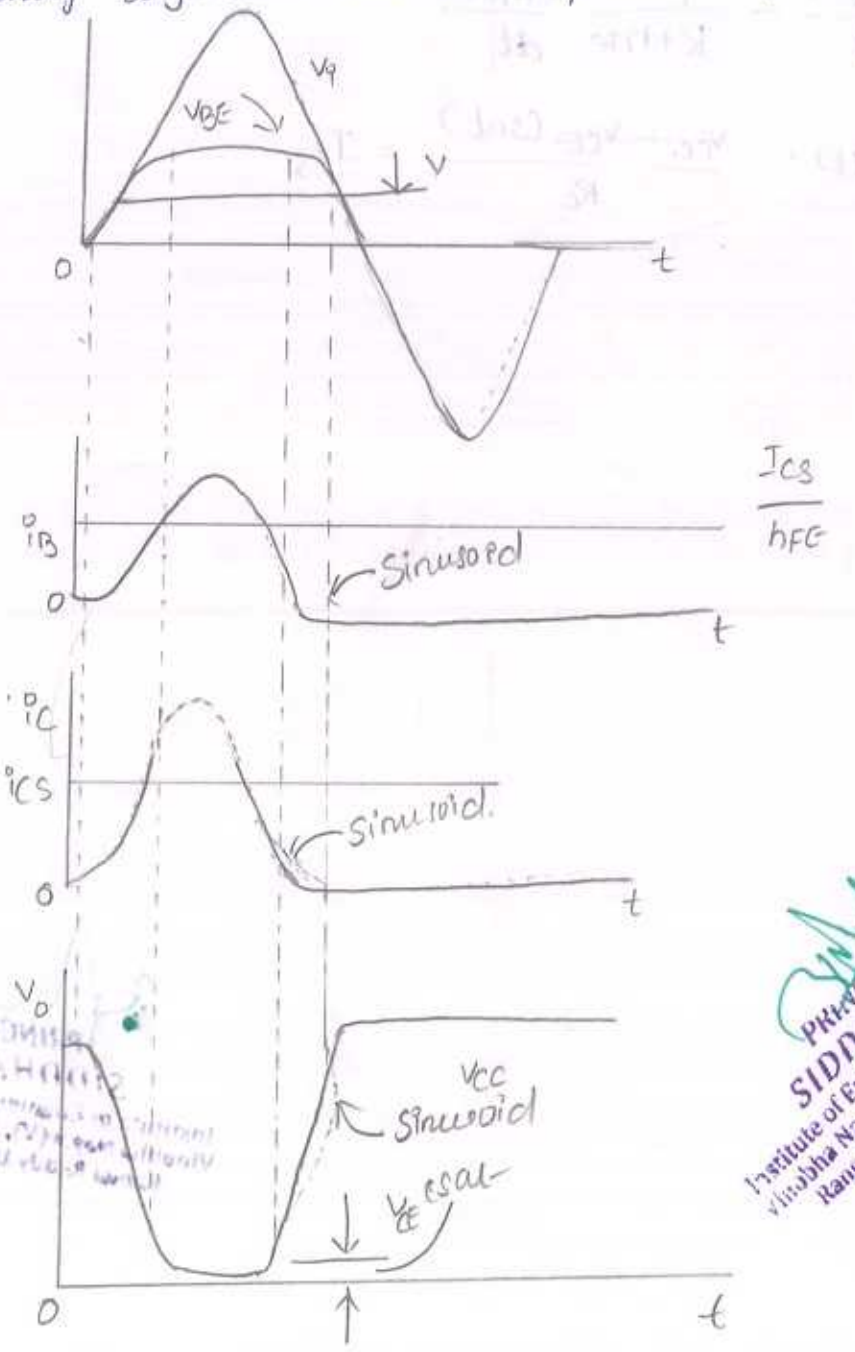


Wave forms of transistor clipper

This limiting occurs when $i_B(t) > I_{CS}/h_{FE}$. The waveforms which result when a sinusoidal voltage $v_i(t)$ carrier the transistor from cut off to Saturation.

2.3 Clipping at Two Independent levels :-

The waveform $i_C(t)$ exhibits clipping at two currents. The clipping levels at which clipping occurs are not independently adjustable but are seperated by the current I_{CS}.

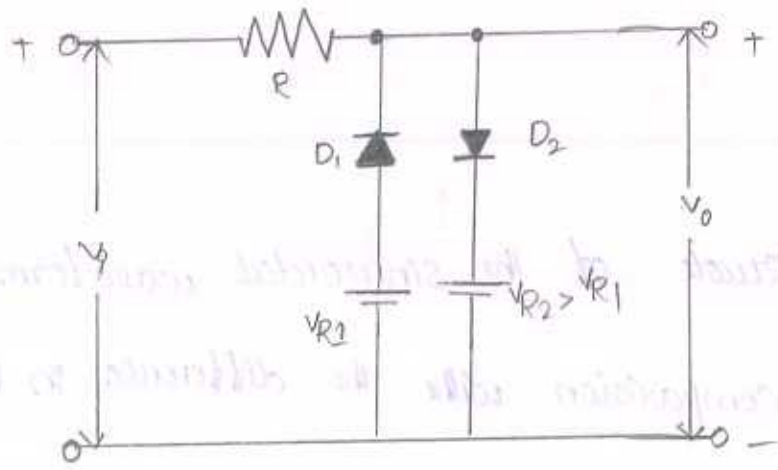


Diode clippers may be used in pairs to perform double-ended limiting at independent levels. A parallel, a Series, or a Series-parallel arrangement may be used.

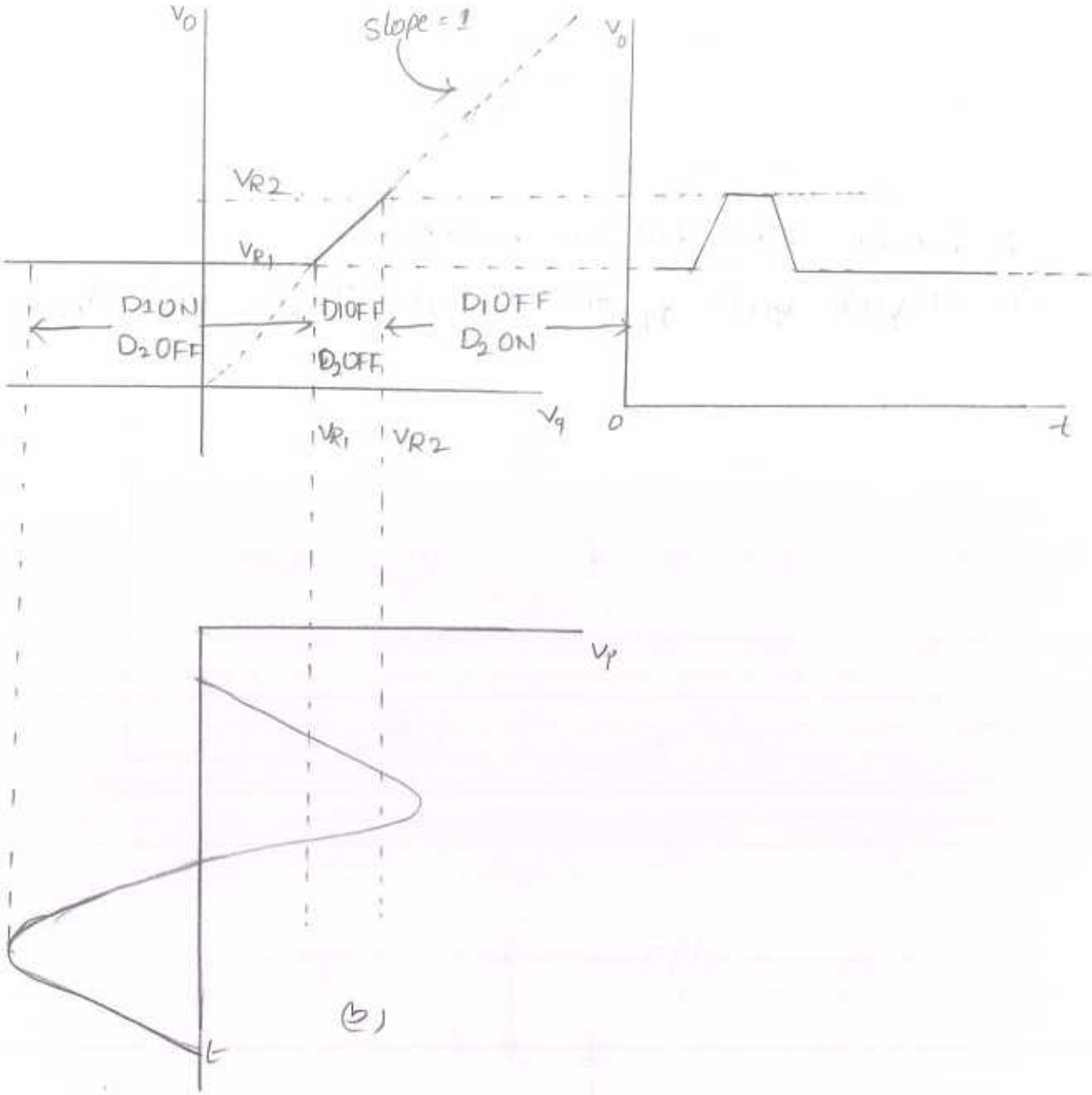
The transfer curve has two breakpoints,

One at $v_0(t) = v_i(t) = V_{R1}$ and a Second at $v_0(t) = v_i(t) = V_{R2}$.

Input $v_i(t)$	Output $v_0(t)$	Diode State
$v_i(t) \leq V_{R1}$	$v_0(t) \leq V_{R1}$	D1 ON, D2 OFF
$V_{R1} < v_i(t) < V_{R2}$	$v_0(t) = v_i(t)$	D1 OFF D2 OFF
$v_i(t) \geq V_{R2}$	$v_0(t) = V_{R2}$	D1 OFF D2 ON



A double-diode clipper, which limits at two independent levels.

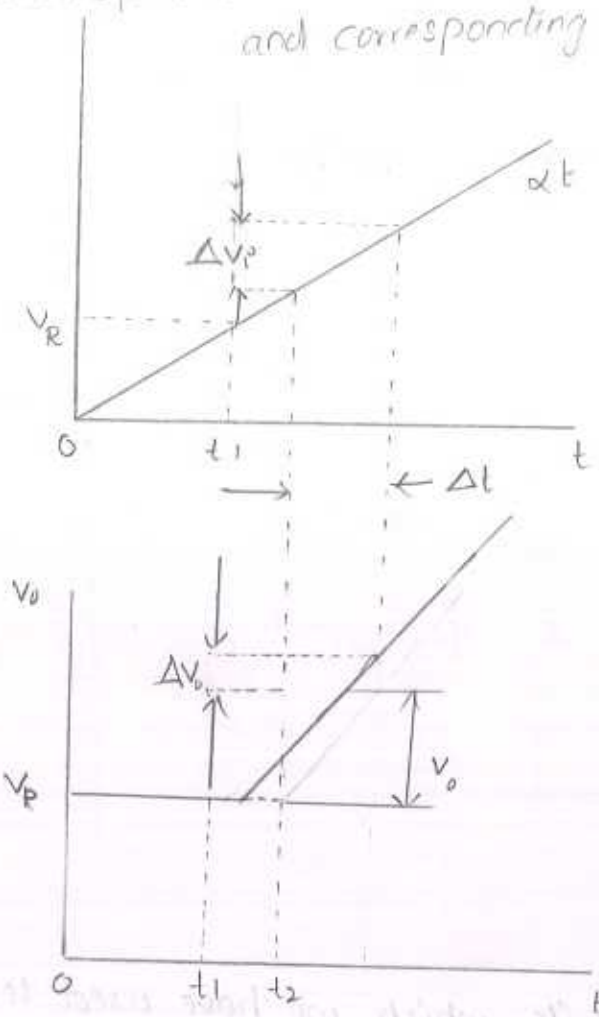


(b)

If the amplitude of the sinusoidal waveform is very large in comparision with the difference in the reference levels, then the output waveform will have been Squared.

→ If the diodes have identical characteristics then clipping symmetrical limiter is obtained..

The comparision operation is illustrated with a ramp input signal $v_i(t)$ and corresponding output waveform is indicated.



The transmission gain $\Delta V_f(t) / \Delta V_i(t) = R/(R+r) = \frac{1}{\beta}$.

The diode actuated by the comparator will respond at a current such that $r = RA$.

The transmission gain between amplifier output and Comparator input is A times that of the diode-resistor combination with $\beta = RA$, or with the amplifier in place.

$$\frac{\Delta V_o(t)}{\Delta V_i(t)} = A\left(\frac{R}{R+r}\right) = \frac{AR}{R+RA} = \frac{A}{1+A}.$$

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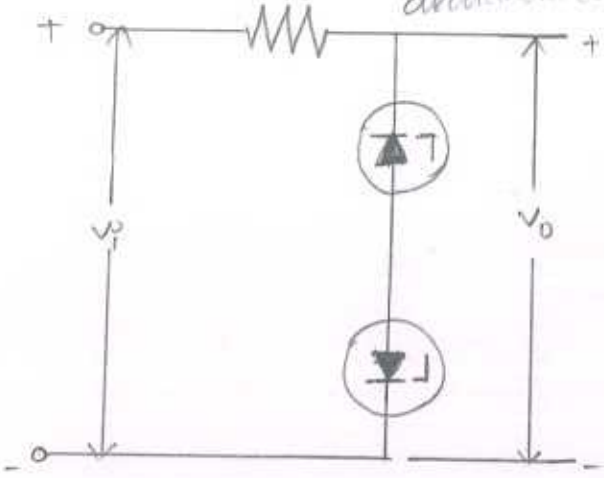
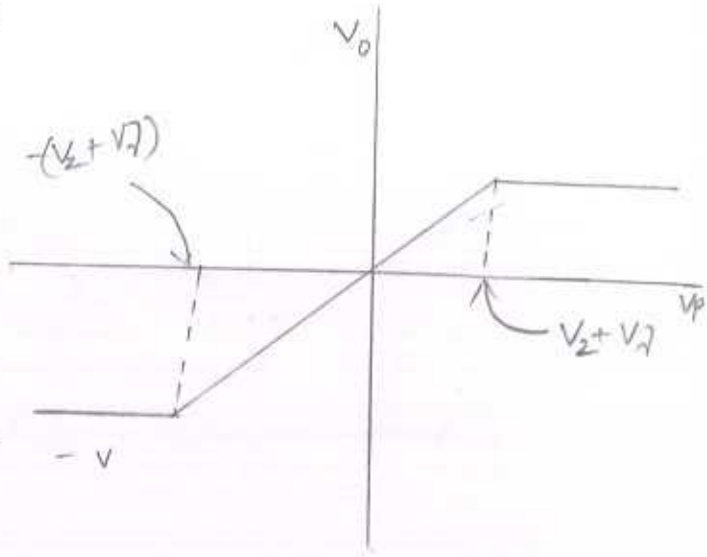
If the breakdown (zener) voltage is V_z and if the cut-in voltage in the forward direction V_γ (≈ 0.5 V for Si), then the transfer characteristics is obtained

A double-ended clipper using avalanche diodes.

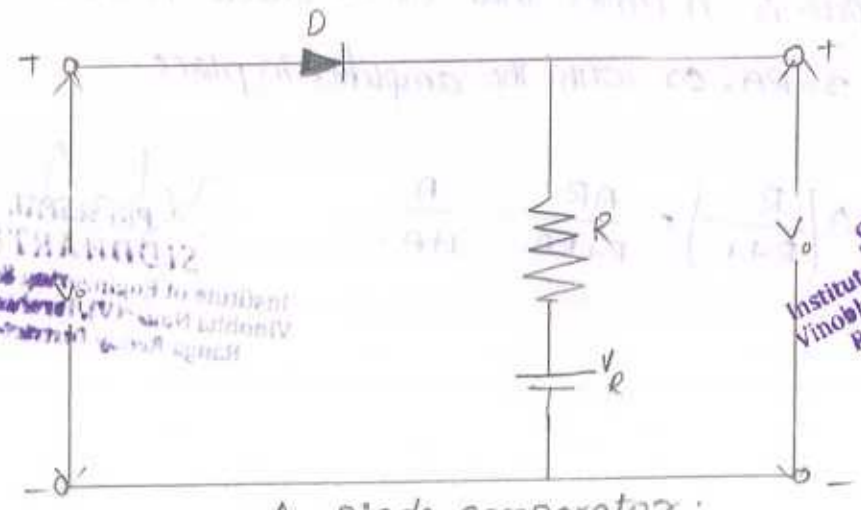


transfer characteristics

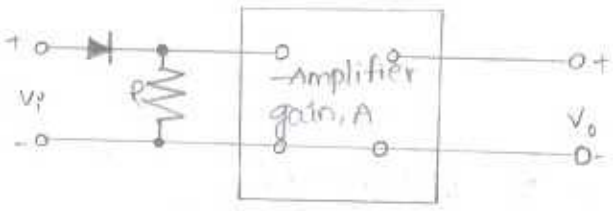


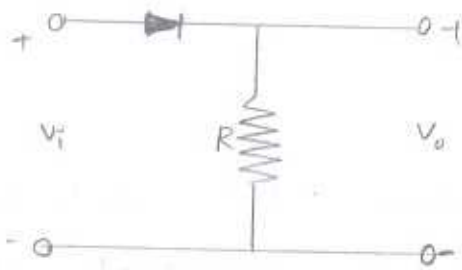
2.4 Comparators :-

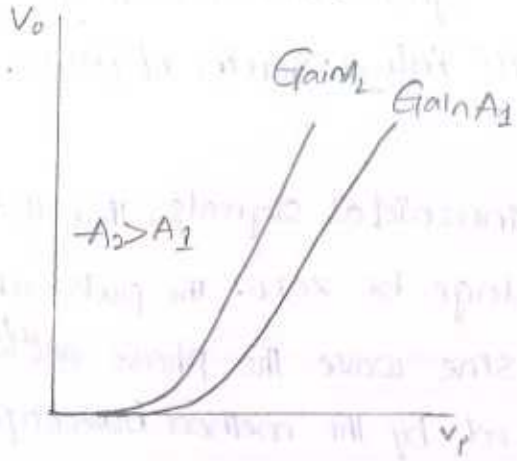
The non linear circuits which we have used to perform the operation of clipping may also be used to perform the operation of comparision. In this case the circuits become elements of a comparator system and are usually referred to simply as comparators.

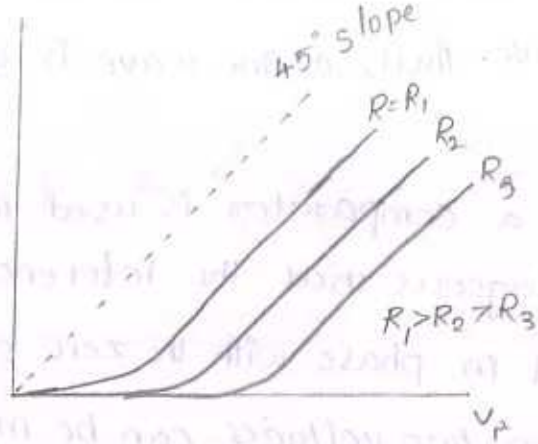


A Diode comparator.









A metal-Semiconductor diode - also called a hot-carrier diode - with the very sharp break in its volt-ampere characteristic, its very low capacitance, and negligible storage time, makes an excellent comparator element.

*2.5 Applications of voltage Comparators:-

The gain of the difference amplifier may be increased by adding more stages. The number of stages, which may be used is limited by the dc stability (drift).

2.5.1 Pulse time modulation:-

If a periodic sweep wave is applied to a comparator whose reference voltage is modulated by some information, it is possible to obtain a succession of pulses whose relative spacing reflects

the input information. The result is a time-modulation system of communication.

2.5.2 Timing markers Generated from a Sine wave:-

If a comparator is used to detect the instant of equality of the instantaneous value of a sine wave with reference voltage, pulses will be obtained which are synchronized with the sine wave. Thus, a sine wave is converted into a sereies of pulses.

2.5.3 Phasemeter:-

When a comparator is used with sinusoidal signals, then it is advantageous that the reference voltage be zero. The pulse are locked in phase with the zero of the sine wave. The phase angle between two voltages can be measured by the method based upon the principle. This time interval is proportional to the phase difference. such a parameter can measure angles from 0 to 360°.

2.5.4 Square-waves from a Sine wave:-

If the comparator output is a signal which assumes either one of the two levels - a step output - then a sine-wave input will result in a square-wave output.

The reference voltage V_R is set equal to zero, then a symmetrical square wave results.

2.5.5 Amplitude-distribution Analyser:-

A comparator is a basic building block in a circuit used to analyse the amplitude distribution of the noise generated in

an active device or the voltage spectrum of the pulses developed by a nuclear-radiation detector, and in similar applications.

2.5 Analog-to-Digital converters:-

It is often required that data taken in a physical system be converted into digital form. Such data would appear in electrical analog form.

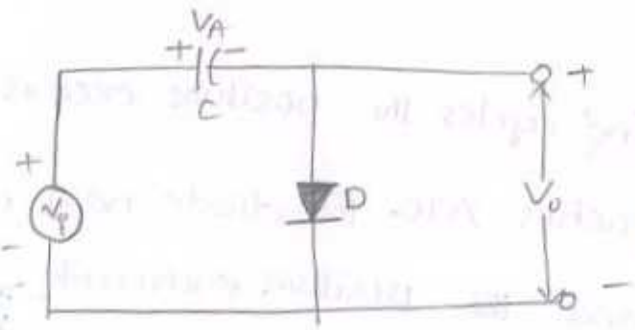
One form of digital voltmeter uses the above-described analog-to-digital converter. The number of pulses that passes through the gate is proportional to the voltage being measured. These pulses go to a counter whose reading is indicated visually by means of LEDs or LCDs.

2.6 The Clamping operation:-

The circuits used to perform this function restrain the extremity of the waveform from going beyond V_R, the circuits are referred to as clamping circuits.

→ A voltage change in only one direction is restrained, the circuits are called one-way clamps. Two diodes may be used to establish a two-way clamp.

The basic circuit of a DC restorer



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Institute of Engineering & Technology,
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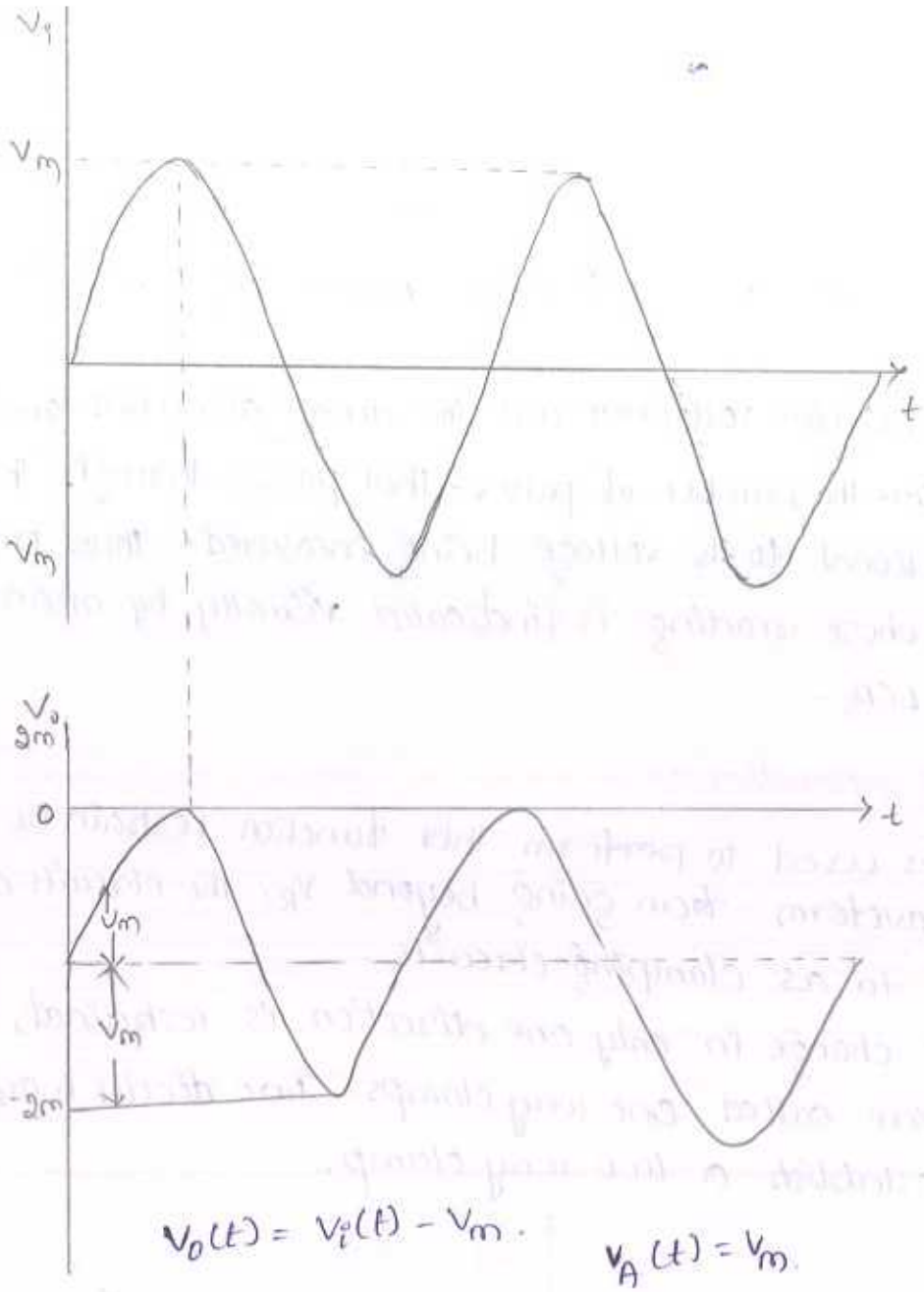
Ranga Reddy District-501 506.

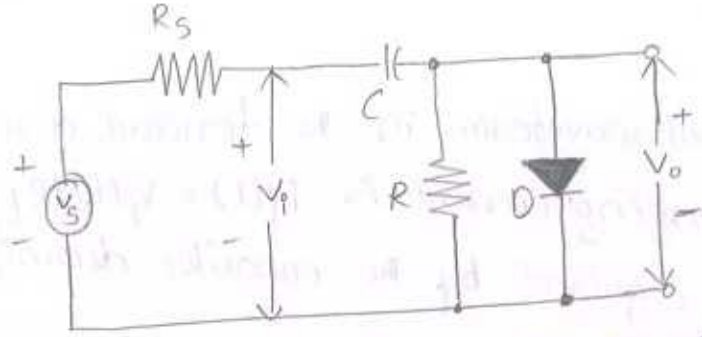


$V_o(t) = V_i(t) - V_m$. $V_A(t) = V_m$.

During succeeding cycles the positive excursion of the signal just barely reaches zero. The diode need never again conduct, and the positive extremity of the signal has been clamped or restored to zero.

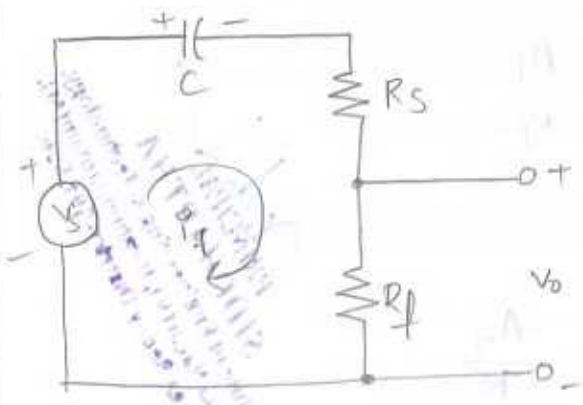
Clamping circuit Taking Source and Diode Resistance into account:-

The resistance R_f will lie in the range tens to hundreds of ohms, depending on the [Source] type of diode used the source resistance may be negligible or may range up to many thousands of ohms depending on the Source.

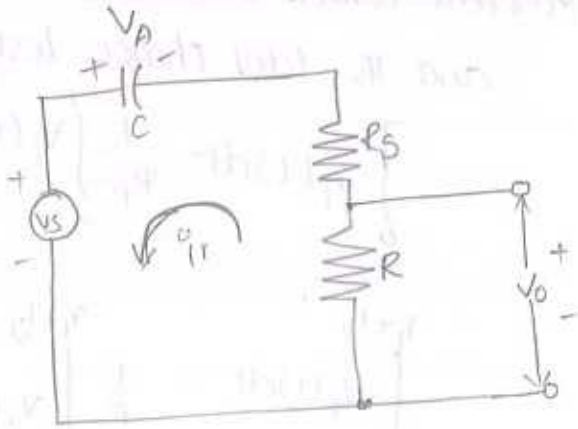


The precision of operation of the circuit depends on the condition that $R >> R_f$.

The Transient wave form:- we wish to follow the wave form, which results after signal is suddenly applied to the circuit. and to see how the steady-state is Reached.



when the diode is conducting



when the diode is not conducting.

It is assumed that $R_f >> R >> R_f$

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2.8 A clamping-circuit theorem:-

In the steady-state, the area A_f under the output voltage waveform in the forward direction - when the diode conducts - is related to the area A_r in the reverse-biased direction - when the diode does not conduct - by the relationship.

$$\frac{A_f}{A_r} = \frac{R_f}{R}$$

If $V_f(t)$ is the output waveform in the forward direction, then, the capacitor charging current is $i_f(t) = V_f(t)/R_f$.
Therefore the charge acquired by the capacitor during the forward interval is

$$\int_0^T i_f(t)\,dt = \frac{1}{R_f}\int_0^T V_f\,dt = \frac{A_f}{R_f}.$$

If $V_r(t)$ is the output voltage in the reverse direction, then the current which discharges the capacitor is $i_r(t) = V_r(t)/R$, and the total charge lost is

$$\int_0^T i_f(t)\,dt = \frac{1}{R_f}\int_0^T V_f(t)\,dt = \frac{A_f}{R_f}$$

$$\int_{T_1}^{T_1+T_2} i_r(t)\,dt = \frac{1}{R}\int_{T_1}^{T_1+T_2} V_r(t)\,dt = \frac{A_r}{R}.$$

29 Practical clamping circuits:

It will normally turn out that $(R_f + R_S)C \ll T_1$ and $(R + R_S)C \gg T_2$

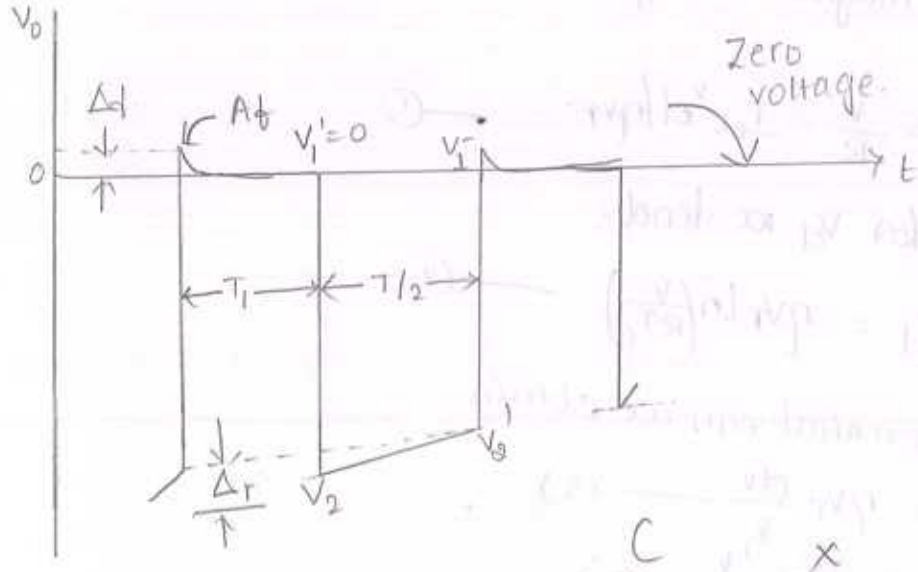
A square-wave or pulse-type waveform, after restoration, typically appears:

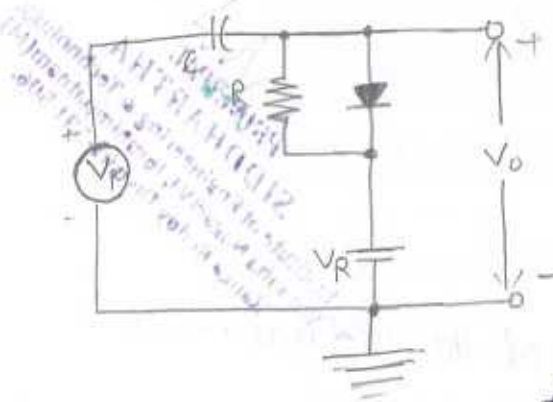
$$V_1' = 0 \quad \text{— (1)}$$

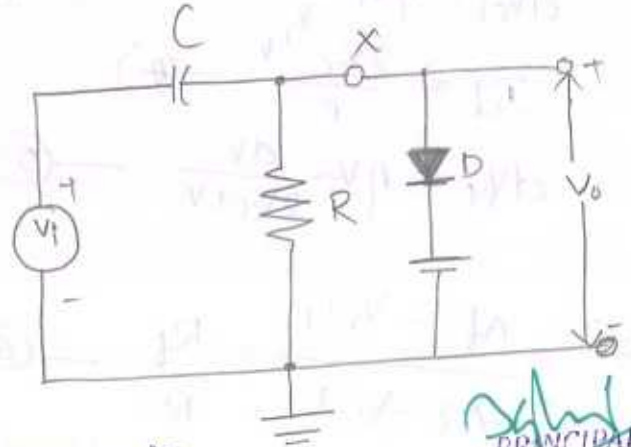
$$V_2 = \frac{R}{R + R_S} V \quad \text{— (2)}$$

$$V_2' = V_2 e^{-T/2 (R+R_S) C} \quad \text{— (3)}$$

$$V_1 = \Delta_f = \left(\frac{R_f}{R_f + R_S}\right)\left(\frac{R + R_S}{R}\right)(V_2' - V_2) \rightarrow (4)$$







$$\frac{A_f - (V_R - V_\gamma)T_1}{A_f} = \frac{R_f}{R}$$

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Q.10 Effect of diode characteristics on clamping voltage :-

The diode as an ideal diode in series with a battery V_f and a resistor R_f

During the interval when the input signal is at its positive extremity v' the diode clamps the output at some clamping voltage V_{cl}, and the corresponding diode current is

$$I_{cl} = I_o e^{V_{cl}/\eta V_T}$$

This current charges the capacitor C so that

$$V_A(t) = V' - V_{cl}$$

The magnitude $V_A(t) - V \leq = V_{cl}$

$$I_{cl} = \frac{V}{R} = I_o e^{V_{cl}/\eta V_T} \quad \text{—①}$$

Solving for V_{cl} we dend.

$$V_{cl} = \eta V_T \ln\left(\frac{V}{R I_o}\right) \quad \text{—②}$$

differential eqn we obtain.

$$dV_{cl} = \eta V_T \frac{dV}{V} \quad \text{— (3)}$$

$$I_{cl} = \frac{2V_{cc} - V}{R} \quad \text{—(4)}$$

$$dV_{cl} = \eta V_T \frac{dV}{2V_{cc} + V} \quad \text{—⑤}$$

$$\frac{A_f - V_f T_1}{A_f - V_{cc} T} = \frac{R_f}{R} \quad \text{—⑥}$$

The peak-to-peak magnitude V of the signal must be larger than $(V_{cc} - V_f)(R_s/R)$.

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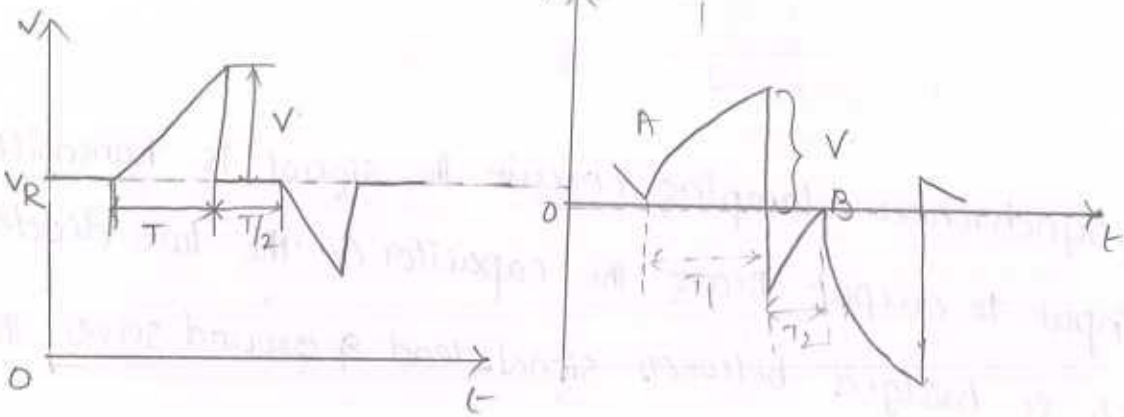
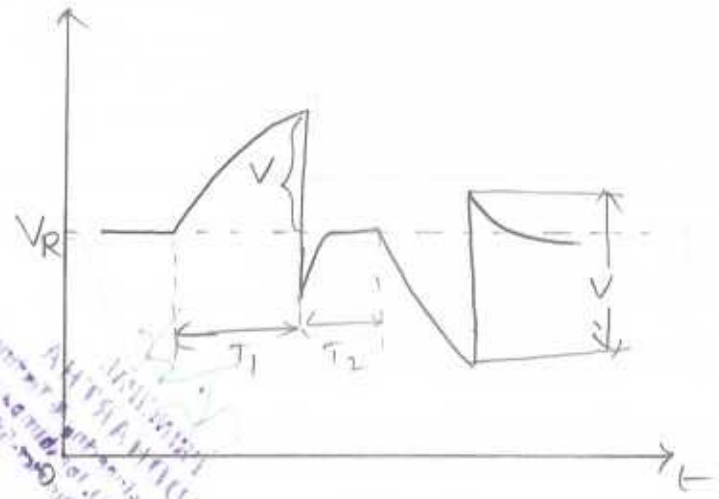
2.11 Synchronized clamping :-

The dc restorers discussed above are examples of clamping circuits in which the time during which the clamping is effective is controlled by the signal itself.

The time of clamping not [con] determined directly by the signal but is determined rather by an auxiliary voltage called a control signal.





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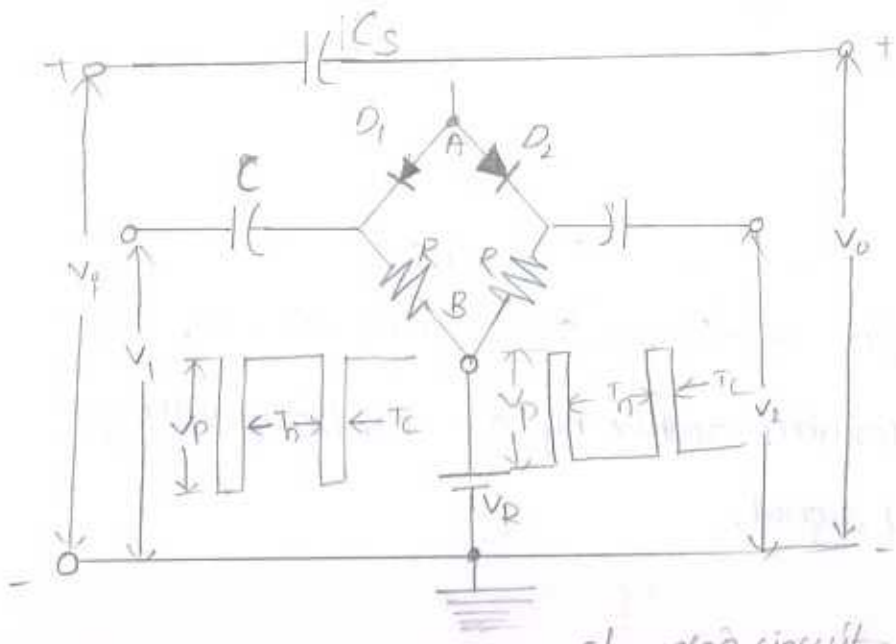

A synchronous clamping circuit.

The Synchronous clamping circuit - The signal is transmitted from input to output through the capacitor C_S. The two diode ckt which is bridged between signal lead & ground serves the function of the switch S.

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STUDENT FEEDBACK ON CURRICULUM

Year	3rd years	Section	A
Academic year	2021 - 2022	semester	I

Give grading to which the syllabus augments course in attaining their defined objectives with
(a) high-3 (b) moderate-2 (c) low-1 (d) poor-0

S.NO	Content	SUB 1	SUB- 2	SUB -3	SUB -4	SUB -5	SUB -6
		MPMC	CS	DCN	COOS	BEFA	
1	Whether the syllabus of the course meets their objectives laid down?	3	3	3	3	3	
2	How well the Teacher explained the Content?						
3	Extent to which the syllabus augments theory with its practical application?	2	2	3	3	3	
4	Does the syllabus meet expected learning values like life skills, human values, gender equality with social response?	.	.	.	.	3	
5	Whether there is relevance between course and the credits offered.	3	3	3	3	3	
6	Whether the elective offered in the curriculum are relevant to your technological aspects?	3	3	3	3	3	
7	Extent to which the syllabus covers all courses that help for higher studies/job opportunities?	3	2	3	2	2	
8	Does the curriculum trains you on critical, logical problem-solving techniques?	3	2	3	3	3	
9	Whether curriculum is providing basic knowledge of technologies related to other domains?	3	3	3	3	3	
	Average						

Any suggestions:

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STUDENT FEEDBACK ON CURRICULUM

Year	III	Section	A
Academic year	2020 - 2021	semester	1

Give grading to which the syllabus augments course in attaining their defined objectives with
(a) high-3 (b) moderate-2 (c) low-1 (d) poor-0

S.NO	Content	SUB 1	SUB- 2	SUB -3	SUB -4	SUB -5	SUB -6
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8	Does the curriculum trains you on critical, logical problem-solving techniques?	2	3	3	2	3	2
9	Whether curriculum is providing basic knowledge of technologies related to other domains?	2	3	3	3	3	3
	Average						

Any suggestions: —

Rajasree
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TEACHER FEEDBACK ON CURRICULUM

Name: T. Nagaraju	**Section:** A
Subject: EMTL	**Year:** II
Academic Year: 2019-20	**Semester:** I

Grade the degree to which the prescribed syllabus and curriculum augments their defined objectives with (a)High-3 (b)Moderate-2 (c)Low-1 (d)Poor-0

S.NO	CONTENT	GRADE
1.	Relevance of text books and reference books to the prescribed syllabus	3
2.	Whether the course content help student to acquire employment	3
3.	Extent the course is framed based in the needs of the follow on courses	2
4.	Whether any relevance between syllabus and course	3
5.	Does the course provide adequate hands on training	2
6.	Extent to which the curriculum requires modern books usage	2
7.	Whether the course content meet industrial requirement	3

COURSE NAME	GAPS IDENTIFIED
EMTL	Vector Analysis

Suggestions if any: —

Signature

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STUDENT FEEDBACK ON CURRICULUM

Year	III	Section	A
Academic year	2020 - 2021.	semester	I

Give grading to which the syllabus augments course in attaining their defined objectives with (a) high-3 (b) moderate-2 (c) low-1 (d) poor-0

S.NO	Content	SUB 1	SUB- 2	SUB -3	SUB -4	SUB -5	SUB -6
1	Whether the syllabus of the course meets their objectives laid down?	3	3	3	3	2	
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4	Does the syllabus meet expected learning values like life skills, human values, gender equality with social response?					2	
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8	Does the curriculum trains you on critical, logical problem-solving techniques?	3	3	2	3	3	
9	Whether curriculum is providing basic knowledge of technologies related to other domains?	3	3	3	3	3	
	Average						

Any suggestions:

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Year	III	Section	A
Academic year	2021 – 2022	semester	I

Give grading to which the syllabus augments course in attaining their defined objectives with (a) high-3 (b) moderate-2 (c) low-1 (d) poor-0

S.NO	Content	SUB 1	SUB- 2	SUB -3	SUB -4	SUB -5	SUB -6
		mpmc	CS	DCN	COOS	DEFA	
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5	Whether there is relevance between course and the credits offered.	3	3	3	3	3	
6	Whether the elective offered in the curriculum are relevant to your technological aspects?	3	3	2	3	3	
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9	Whether curriculum is providing basic knowledge of technologies related to other domains?	3	3	3	3	2	
	Average						

Any suggestions:

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Year	III	Section	A
Academic year	2021-2022	semester	I

Give grading to which the syllabus augments course in attaining their defined objectives with
(a) high-3 (b) moderate-2 (c) low-1 (d) poor-0

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	Average						

Any suggestions: ———

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STUDENT FEEDBACK ON CURRICULUM

Year	III	Section	A
Academic year	2021 – 2022	semester	I Semester

Give grading to which the syllabus augments course in attaining their defined objectives with (a) high-3 (b) moderate-2 (c) low-1 (d) poor-0

S.NO	Content	SUB 1 MPMC	SUB- 2 CS	SUB -3 DCN	SUB -4 COOS	SUB -5 BEFA	SUB -6
1	Whether the syllabus of the course meets their objectives laid down?	3	2	3	3	3	
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Any suggestions:

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STUDENT FEEDBACK ON CURRICULUM

Year	3rd	Section	'A'
Academic year	2021 – 2022	semester	I

Give grading to which the syllabus augments course in attaining their defined objectives with
(a) high-3 (b) moderate-2 (c) low-1 (d) poor-0

S.NO	Content	SUB 1	SUB- 2	SUB -3	SUB -4	SUB -5	SUB -6
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	Average						

Any suggestions:

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B. Deekshitha
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	Vinoba Nagar, Ibrahimpatnam, R.R Dist.	SIET/ACA/F-05
	SYLLABUS COVERAGE REPORT	Rev.00

Department: ECE **Class/ Sem : III-I -A**

Month & Year: Jan 2021 **Date: 05/01/2021**

Sl. No.	Name of the Subject/Lab	Name of the Faculty	No. of units /Experiments covered (Cumulative)	Planning if short fall	Faculty Sign
1.	DCN	Mrs. N. Malathi	unit 1,2,3,4 – completed Unit 5 – 50% completed	–	
2.	CS	Mr. T. Mohan Rao	1,2,3,4 - Units completed Unit - 5 - 80% completed		Mohan
3.	MPMC	Dr. T. Krishnarjuna Rao	unit-5 50% completed		
4.	BEFA	Mr. V. Ramesh	Unit-5 completed (5 units)		Ramesh
5.	COOS	Dr. V. Vasavi	Unit-5 - 60% Completed		Vasavi
6.	EMI	Dr. Farha Anjum	unit - V 75% done	-	Farha
7.	DCN LAB	Mrs. N. Malathi/ Mrs. R. Sunitha	9 experiments finished	will complete in time	Malathi
8.	MPMC LAB	Dr. T. Krishnarjuna Rao	10 Expts Completed		
9	AECS LAB	Mrs. Nagabhavani	4 experiments done	-	Bhagi

Farha

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S. Krishna

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	Vinoba Nagar, Ibrahimpatnam, R.R Dist.	SIET/ACA/F-05
	SYLLABUS COVERAGE REPORT	Rev.00

Department: ECE **Class/ Sem : III-I-B**

Month & Year: Jan 2021 **Date: 05/01/2021**

Sl. No.	Name of the Subject/Lab	Name of the Faculty	No. of units /Experiments covered (Cumulative)	Planning if short fall	Faculty Sign
1.	DCN	Mrs. N. Malathi	1,2,3,4 completed unit - 5 - 50% completed	-	
2.	CS	Mr. T. Mohan Rao	1, 2, 3, 4 completed unit - 5 - 80% completed		
3.	MPMC	Dr. T. Krishnarjuna Rao	Unit - 5 - 80% Completed		
4.	BEFA	Mr. V. Ramesh	5 Units Completed (All)		
5.	COOS	Dr. V. Vasavi	Unit - 5 - 60% completed		Vasavi
6.	EMI	Dr. Farha Anjum	unit - V 60% done		Farha
7.	DCN LAB	Mrs. N. Malathi/ Mrs. R. Sunitha	9 experiments finished	will complete in time	Malathi
8.	MPMC LAB	Dr. T. Krishnarjuna Rao	10 Experiments Completed		
9	AECS LAB	Mrs. Nagabhavani	4 experiments done	-	

Farha

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Ranga Reddy District-501 506.

S. Krishna Rao

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Vinoba Nagar, Ibrahimpatnam, R.R. Dist. 501506

	Vinoba Nagar, Ibrahimpatnam, R.R Dist.	SIET/ACA/F-05
	SYLLABUS COVERAGE REPORT	Rev.00

Department: ECE **Class/ Sem : IV-I -B**

Month & Year: Jan 2021 **Date: 05/01/2021**

Sl. No.	Name of the Subject/Lab	Name of the Faculty	No. of units /Experiments covered (Cumulative)	Planning if short fall	Faculty Sign
1.	MWOC	Mr.T. Nagaraju	V-unit 50% completed		
2.	DS	Mr. K. Pavani	V unit – 75% completed		Pavani
3.	DBMS	---			
4.	PPLE	Mrs. G. Deepthi	unit-5-60% done –		Deepthi
5.	SL	Mr. Saiteja	V-unit 50% completed		
6.	DIP	G.Sai Ram	V-Unit 70% completed		
7.	MWOC Lab	Mr.T. Nagaraju/ G.Sai Ram	10 experiments completed		

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	SYLLABUS COVERAGE REPORT	Rev.00

Department: ECE **Class/ Sem : IV-I -A**

Month & Year: Jan 2021 **Date: 05/01/2021**

Sl. No.	Name of the Subject/Lab	Name of the Faculty	No. of units /Experiments covered (Cumulative)	Planning if short fall	Faculty Sign
1.	MWOC	Mr.T. Nagaraju	IV unit 50% Completed		
2.	DS	Mr. K. Pavani	V unit - 70% completed	-	Pavani
3.	DBMS	---			
4.	PPLE	Mrs. G. Deepthi	unit - 5 - 60% done	-	Deepthi
5.	SL	Mr. Saiteja	V - unit 50% completed		
6.	DIP	G.Sai Ram	V-Unit 70% completed		
7.	MWOC Lab	Mr.T. Nagaraju/ G.Sai Ram	10 experiments completed		

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Ranga Reddy District-501 506.

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